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# Intel Sky Lake Platform

## SLK-S CPU / SLK PCH-H

### Project Information

Phase: SMVB

Ver:1.00

SVID: 103C

SSID: 82C9


Form factor:uATX

Project	Description	PCA PN	SCH PN (DG#)	PCB PN	ASSY CODE
OLAF	MBD,Olaf,Intel,skylake,H110,SFF	901279-001	TBD	TBD	FYVH

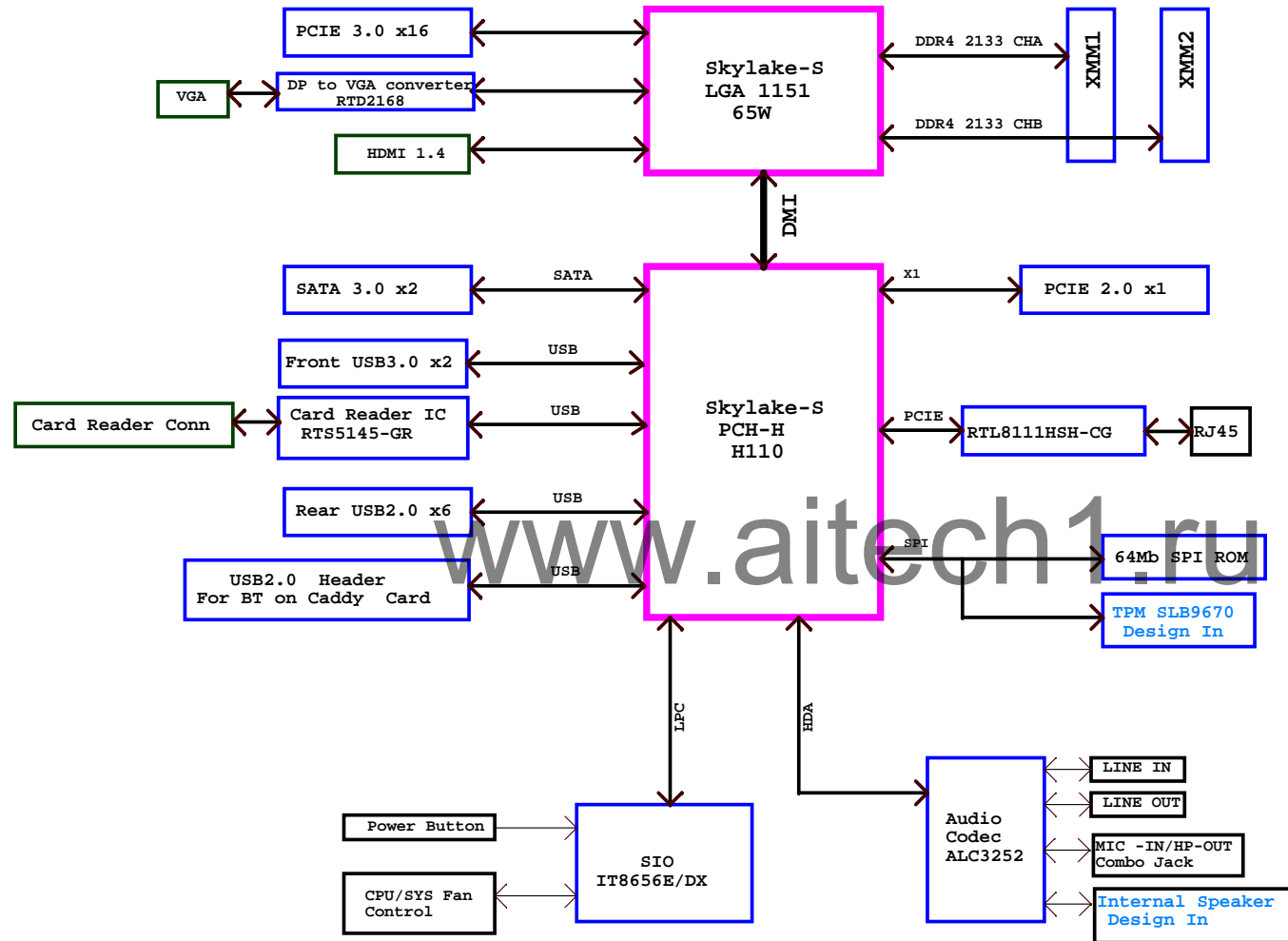
Marking	Description
I	Installed
NI	Not Installed
MP	Production Part ONLY
PROTO	Not For Production Part
CCL	Critical Components List

PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
DB	RED	YELLOW
SI	LIGHT BLUE	WHITE
PV/SMVB	GREEN	WHITE

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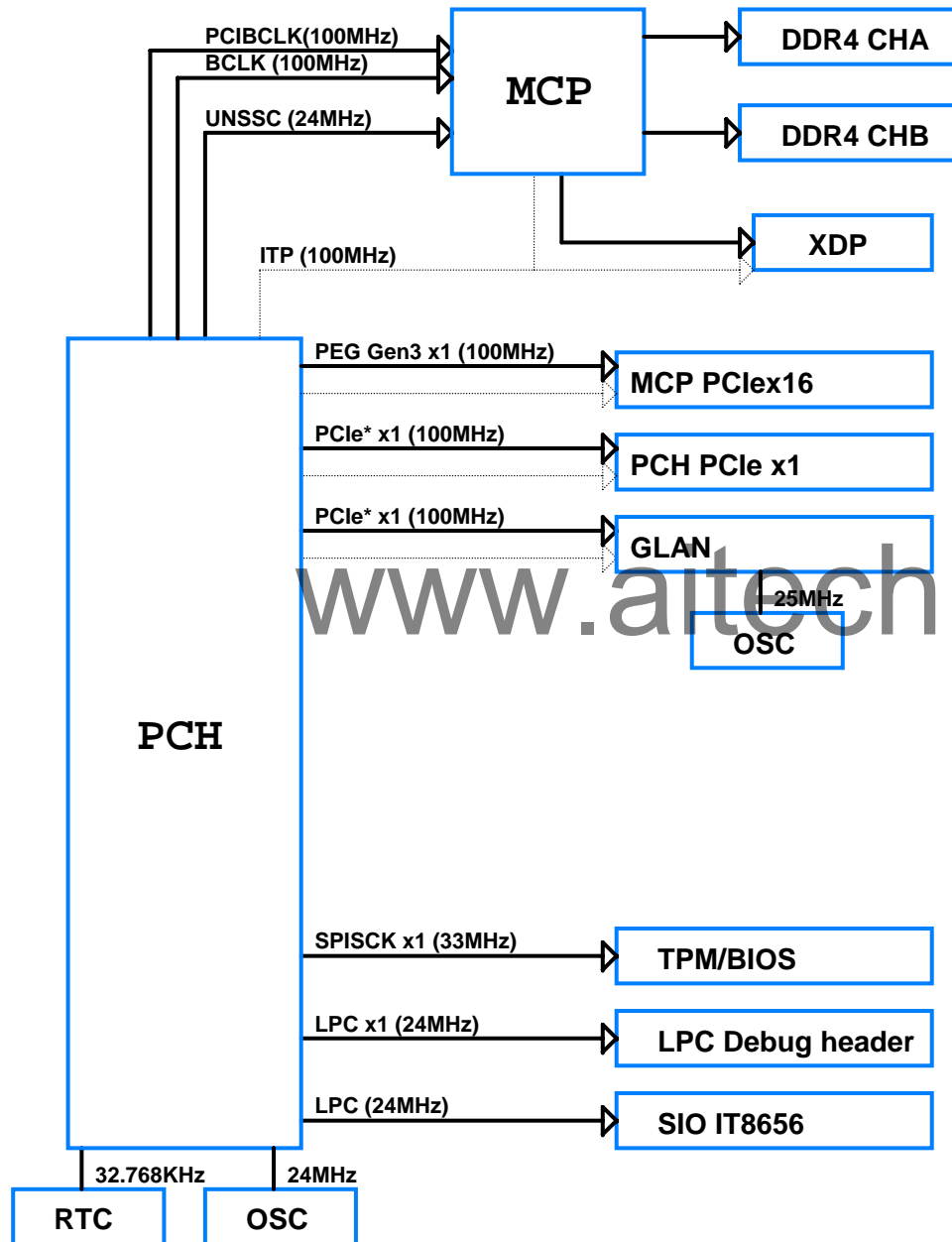
# System BLOCK Diagram




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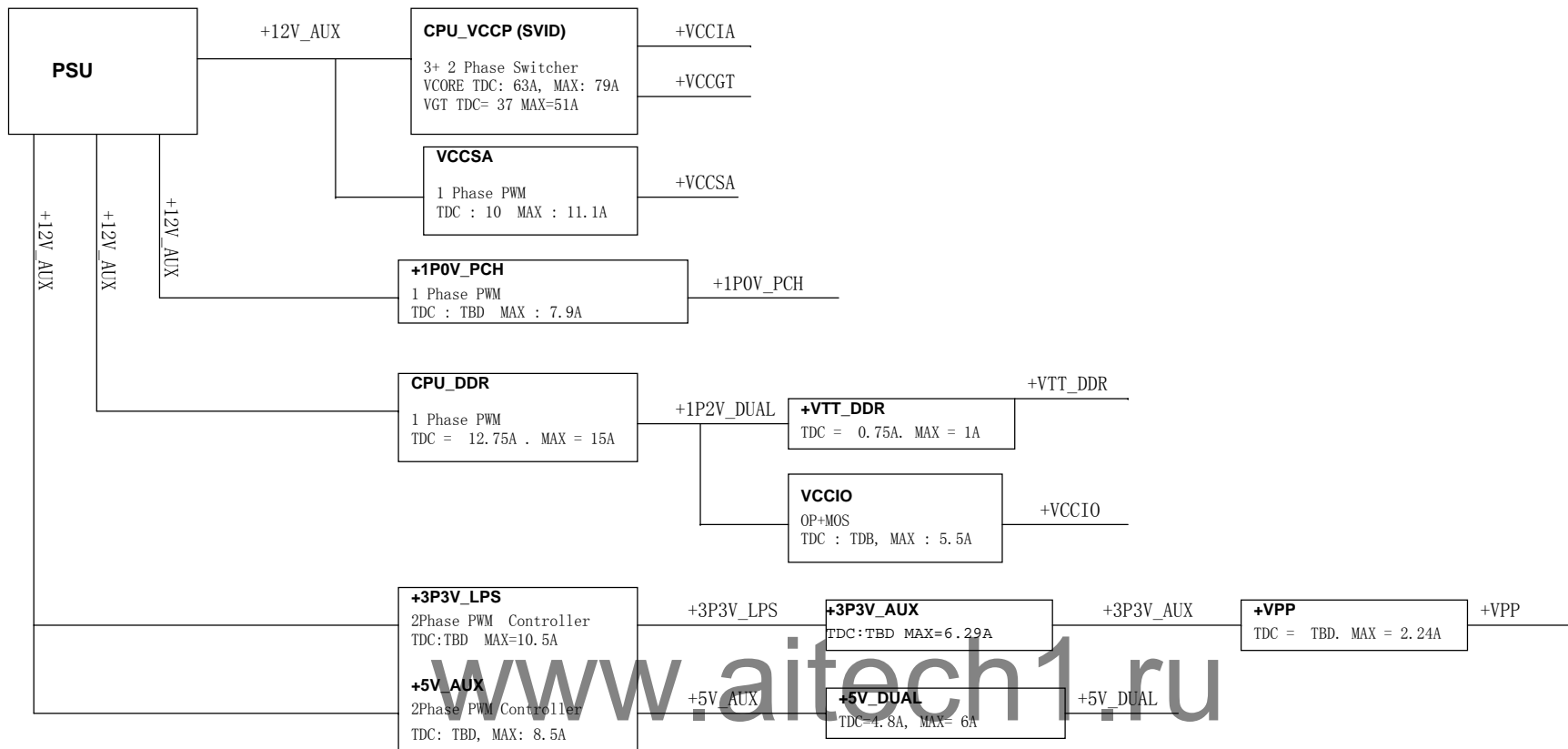
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# Clock Diagram



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**VBAT 3.0**  
VCCRTC

BATT1	
+VCCIA	70A
+VCCGT	37A
+VCCIO	5.5A
+VCCSA	11A
+1P2V_DUAL	2.8A

DDR4 DIMM x2	
+VTT_DDR	1A 0.75W
+1P2V_DUAL	10.8A 12.96W
VPP	2.24A 5.6W

SUPER I/O	
+3P3V	15mA 49.5mW
+3P3V_LPS	20mA 66mW
+3V_BATT	1uA 3.3uW

AUDIO	
+5V_AUX	570mA 2.85W
+3P3V_AUX	80mA 0.264W

SPI ROM	
+3P3V_AUX	30mA 0.1W

USB PORT x9	
3.0 X 2(1.8A)	
2.0 X6(3A)	
Card Reader(0.4A)	5.2A 26W

FAN	
+12V	200mA 2.4W

LAN	
+3P3V_LAN	0.125A 0.412W

DP2VGA	
+3P3V	0.18A 0.6W

TPM	
+3P3V_AUX	25mA 85mW

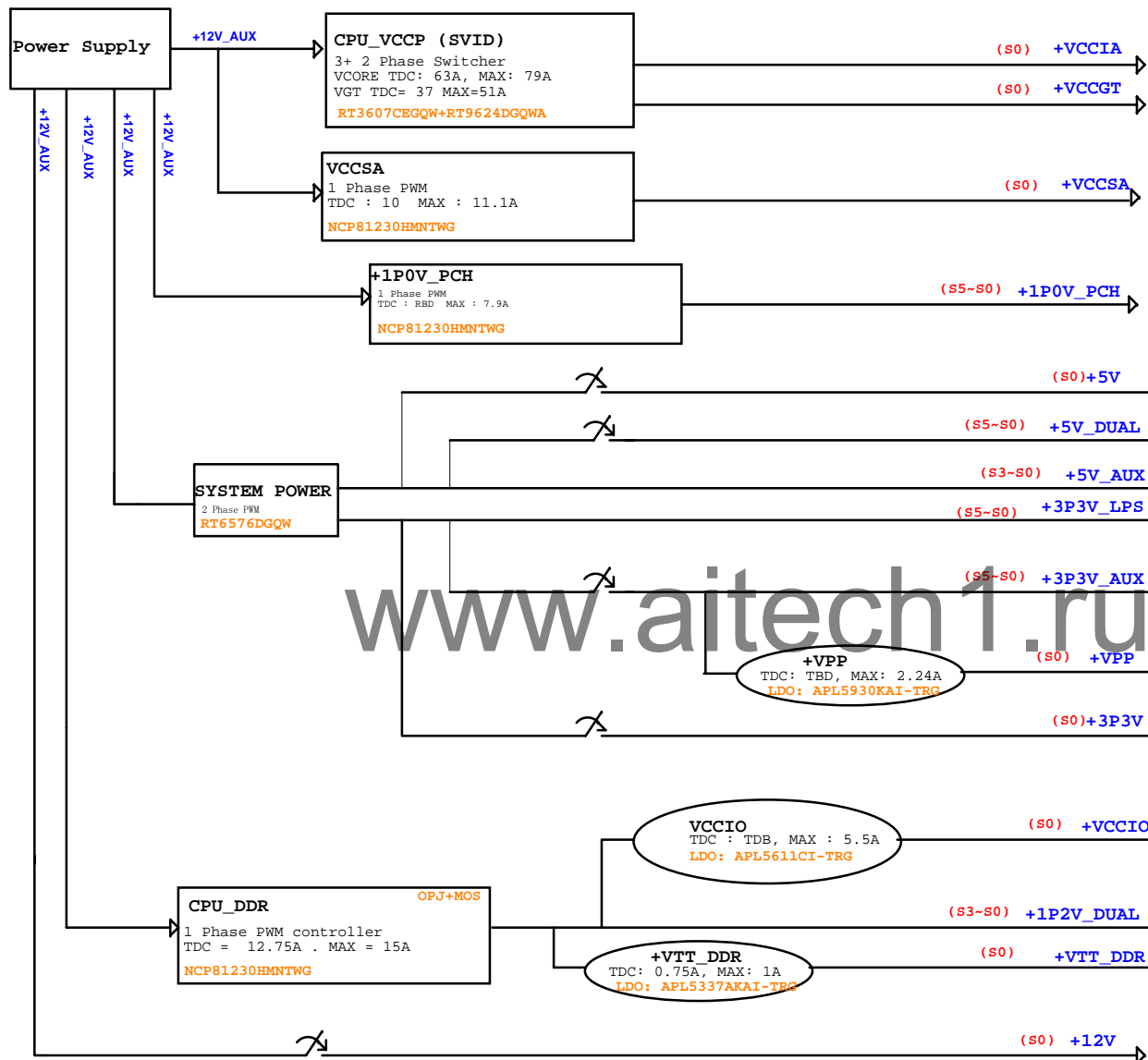
HDD/ODD Power	
HDD	
+12V 0.6A 7.2W	
+5V 0.7A 3.5W	
ODD	
+12V 2A 24W	
+5V 1.5A 7.5W	

PCIEX1	
+3P3V	3A 10W
+12V	0.5A 6W
+3P3V_AUX	0.375A 1.24W

PCIEX16	
+3P3V	3A 10W
+12V	3A 36W
+3P3V_AUX	0.375A 1.24W
TDP 30W	

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Title <b>POWER DISTRIBUTION DIAGRAM</b>									
Size	Document Number				Rev				
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Title: <b>POWER FLOW</b>			
Size: <b>TBD</b> Custom: <b>TBD</b>	Document Number: <b>TBD</b>		Rev: <b>0A</b>
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## PCH GPIO

Device	Power supply	Default voltage	Native resolution	Default status	Actual Power Mode	Actual voltage	Image/IO/CMOS	Native vs SPD	Resolution	Bit/Hz
OPP_A0	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	PW 10K to 55	+VSPD_A0/A1	Reserve SPD_A0B0ST-MS00	Native	NA	NA
OPP_A1	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A01	Native	NA	NA
OPP_A2	1.80 V 3.3V	LTC module: L401 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A02	Native	NA	NA
OPP_A3	1.80 V 3.3V	LTC module: L402 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A03	Native	NA	NA
OPP_A4	1.80 V 3.3V	LTC module: L403 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A04	Native	NA	NA
OPP_A5	1.80 V 3.3V	LTC module: L404 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A05	Native	NA	NA
OPP_A6	1.80 V 3.3V	LTC module: L405 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	LTC_A06	Native	NA	NA
OPP_A7	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	PW 10K to 55	+VSPD_A7	SSR_A07	Native	NA	NA
OPP_A8	1.80 V 3.3V	LTC module: CL0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	PW 10K to 55	+VSPD_A8/A9	NA	NA	NA	NA
OPP_A9	1.80 V 3.3V	LTC module: CL0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	CL0000_A09	Native	NA	NA
OPP_A10	1.80 V 3.3V	LTC module: CL0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	CL0000_A10	Native	NA	NA
OPP_A11	1.80 V 3.3V	LTC module: PR0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	PW 20K to 55	+VSPD_A11	SC0000_A011	SPM	NA	NA
OPP_A12	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	PW 10K to 55	+VSPD_A12/A13	NA	NA	NA	NA
OPP_A13	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	SC0000_A013	NA	NA	NA
OPP_A14	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	NA	NA	NA	NA	NA	NA
OPP_A15	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native	NA	PW 10K to 55	+VSPD_A15/A16	SC0000_A015	Native	NA	NA
OPP_A16	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	Native vs SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A17	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A18	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A19	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A20	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A21	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A22	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A23	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A24	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_A25	1.80 V 3.3V	LTC module: RCH0000 APPL module: ESP_A0_B0ST-MS00	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B0	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B1	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B2	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B3	1.80 V 3.3V	None	SPM	NA	PW 10K to 55	+VSPD_A0/A1	NA	NA	NA	NA
OPP_B4	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B5	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B6	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B7	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B8	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B9	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B10	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B11	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B12	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B13	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B14	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B15	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B16	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B17	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B18	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B19	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B20	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B21	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B22	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B23	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B24	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_B25	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C0	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C1	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C2	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C3	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C4	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C5	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C6	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C7	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C8	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C9	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C10	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C11	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C12	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C13	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C14	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C15	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C16	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C17	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C18	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C19	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C20	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C21	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C22	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C23	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C24	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_C25	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D0	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D1	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D2	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D3	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D4	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D5	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D6	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D7	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D8	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D9	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D10	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D11	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D12	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D13	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D14	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D15	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D16	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D17	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D18	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D19	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D20	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D21	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D22	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D23	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D24	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_D25	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E0	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E1	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E2	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E3	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E4	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E5	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E6	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E7	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E8	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E9	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E10	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E11	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E12	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E13	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E14	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E15	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E16	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E17	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E18	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E19	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E20	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E21	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E22	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E23	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E24	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_E25	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F0	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F1	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F2	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F3	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F4	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F5	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F6	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F7	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F8	1.80 V 3.3V	None	SPM	NA	NA	NA	NA	NA	NA	NA
OPP_F9	1.80 V 3.3V	None	SPM	NA	NA					

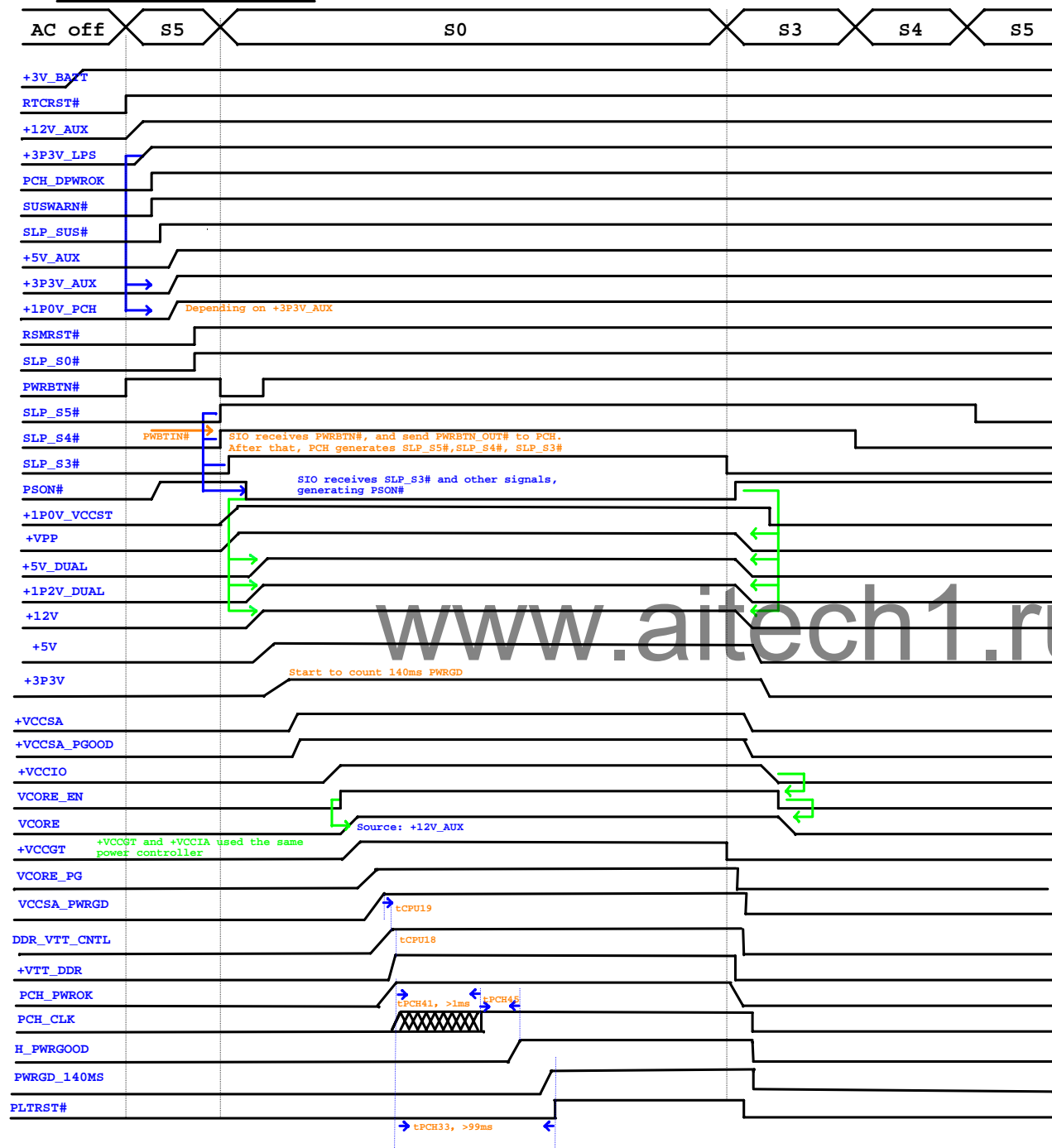
## PCH GPIO

[illegible]

## SIO GPIO

[illegible][illegible]

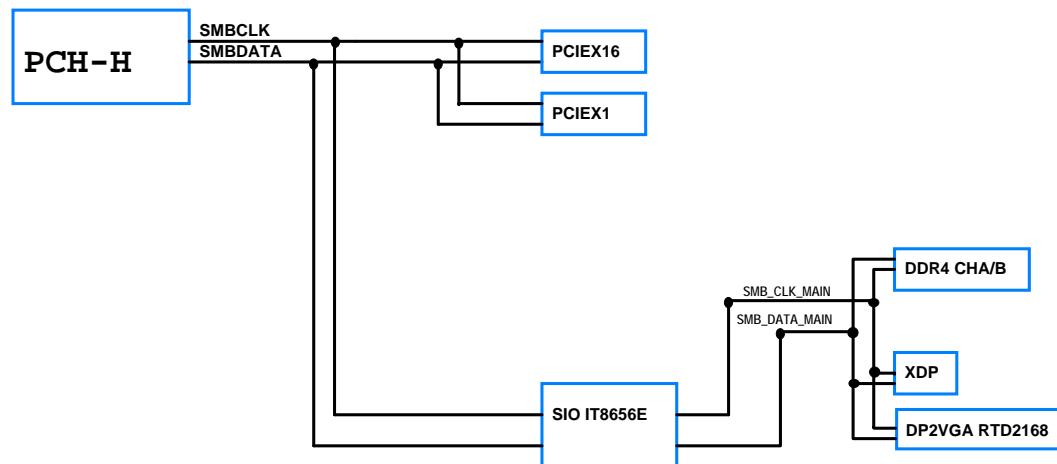
# POWER SEQUENCE DIAGRAM



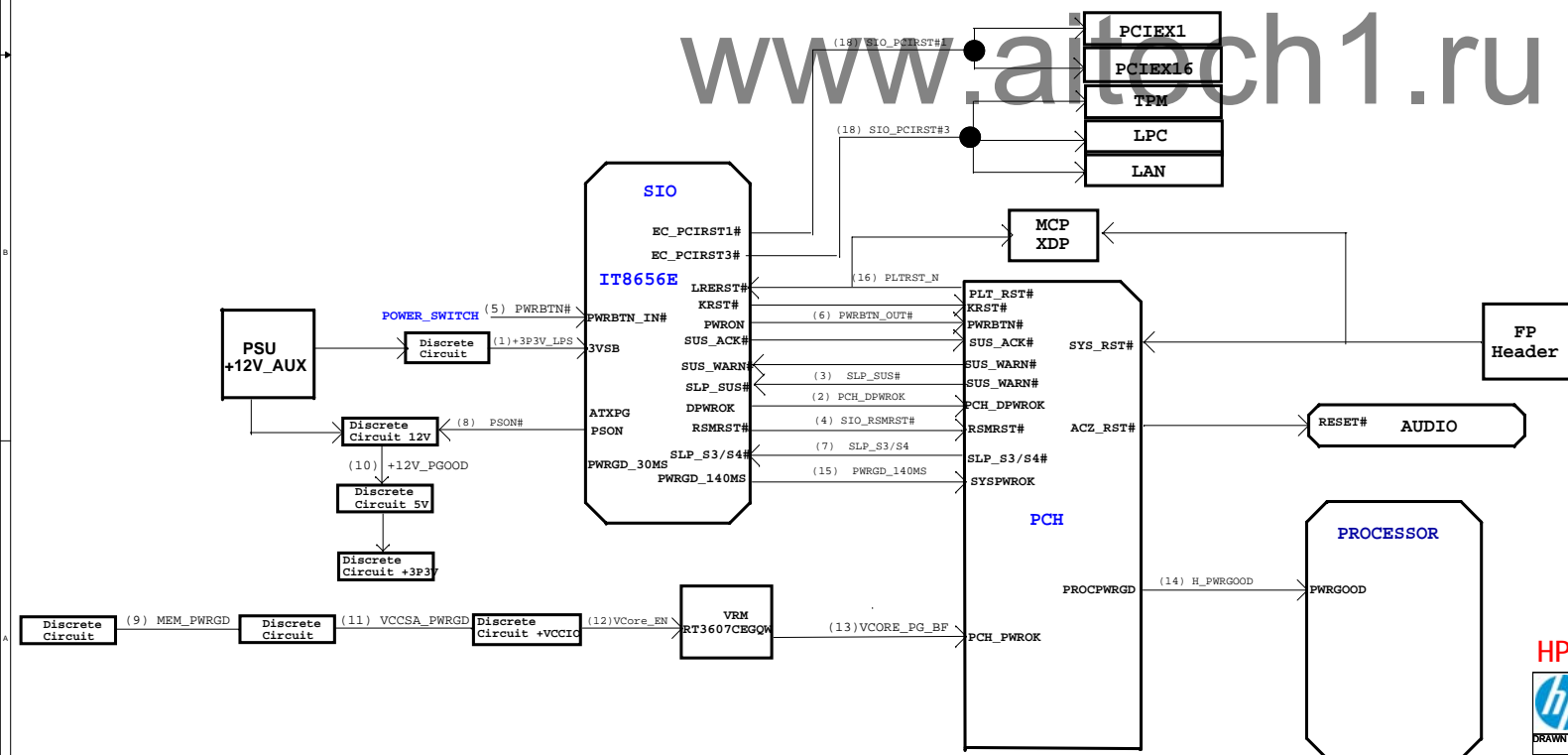
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Title: <b>POWER SEQUENCE DIAGRAM</b>			
Size: <b>C</b>	Document Number: <b>TBD</b>	Rev: <b>0A</b>	
Date: <b>Thursday, July 14, 2016</b>		Sheet: <b>7</b>	of: <b>82</b>

# SM Bus MAP



# RESET/PWROK MAP



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Title: <b>SMBUS/PGOOD/RESET DIAGRAM</b>			
Size: <b>C</b>	Document Number: <b>TBD</b>	Rev: <b>0A</b>	
Date: <b>Thursday, July 14, 2016</b>		Sheet: <b>8</b>	of: <b>82</b>



The schematic diagram illustrates the power supply section of the board. It features several +1P0V\_VCCST power supply pins. The H\_TMS and H\_TDI signals are connected to the power supply through resistors R236 and R235, respectively. The CPU\_FREQ\_N signal is connected to the power supply through resistor R116. The H\_TDO signal is connected to the power supply through resistor R117. The H\_TRST# signal is connected to the power supply through resistor R796. The H\_TCK signal is connected to the power supply through resistor R152. The H\_TCK1 signal is connected to the power supply through resistor R891. A 100nF capacitor C70 and a 16V tantalum capacitor X7R\_16V are also shown connected to the power supply.

**Intel MCP XDP Debug Connector**

PRDY# and PREQ# must connect for DCI Merged Debug Port Topology

DB2

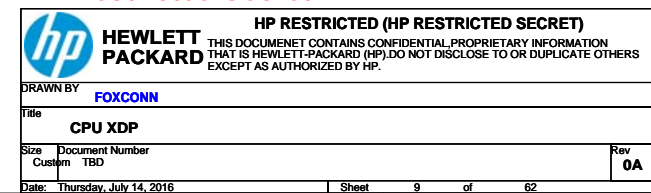
Place near CPU within 500mils

Place near PCH within 500mils (SPI\_I02)  
R93 near PCH within 110mils (SPI\_MOSI\_R)

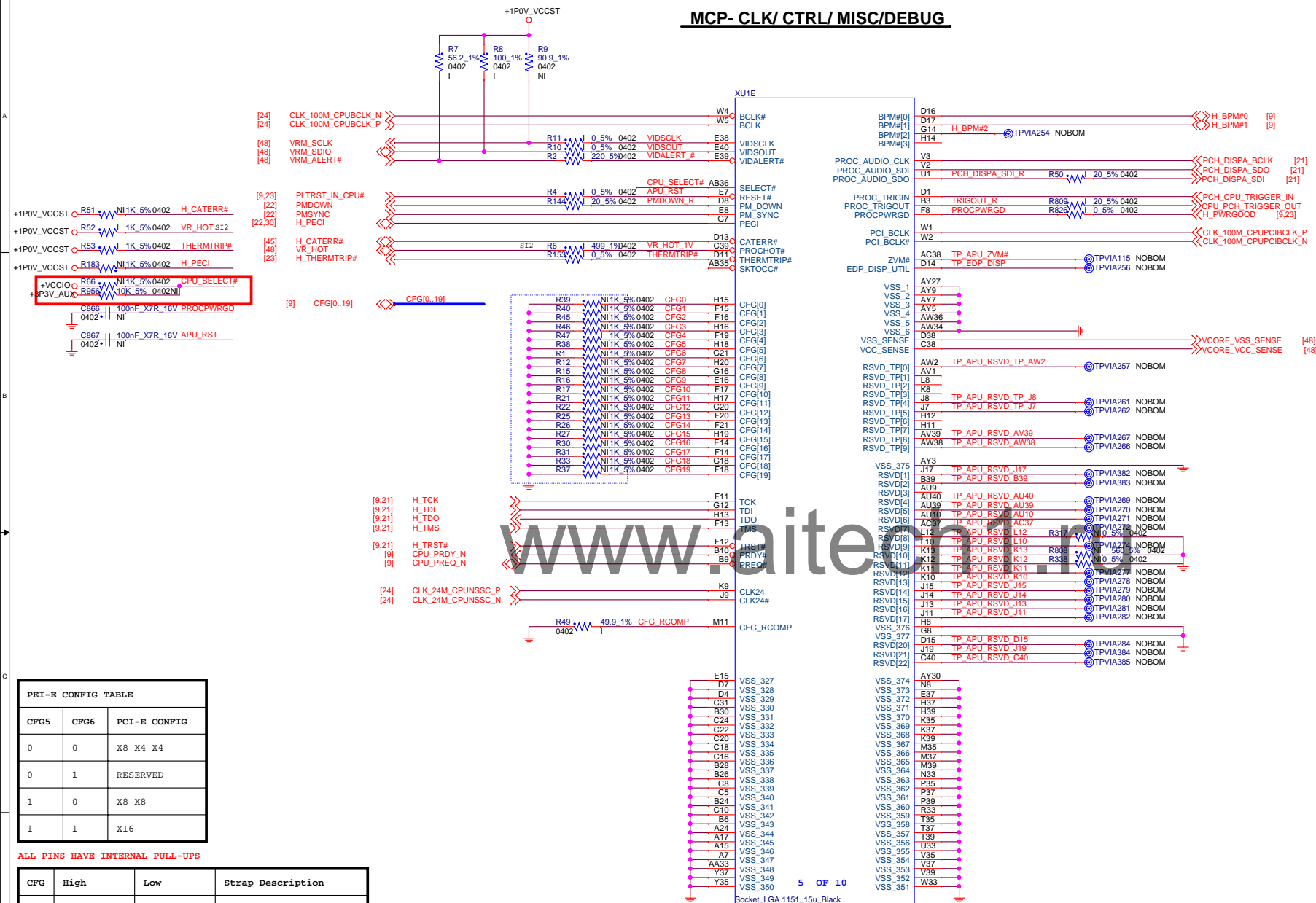
Note:  
VCCST Power Gating (Q1) implemented: XDP\_PRESENT# need connect to Q1.G with a inverse logic.

PV to SMVB (20160624):  
1. Change P4 footprint from HMS2X30CZ to HMS2X30CZ\_MVB\_NP  
Add slider marker on XDP pin

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## MCP- CLK/ CTRL/ MISC/DEBUG



PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

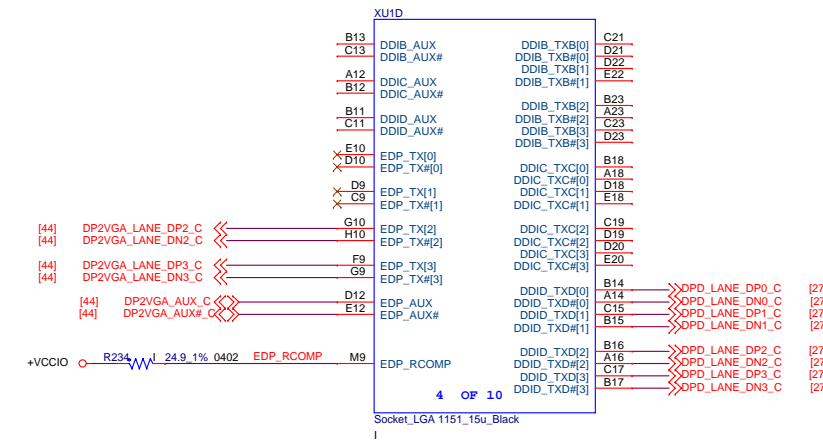
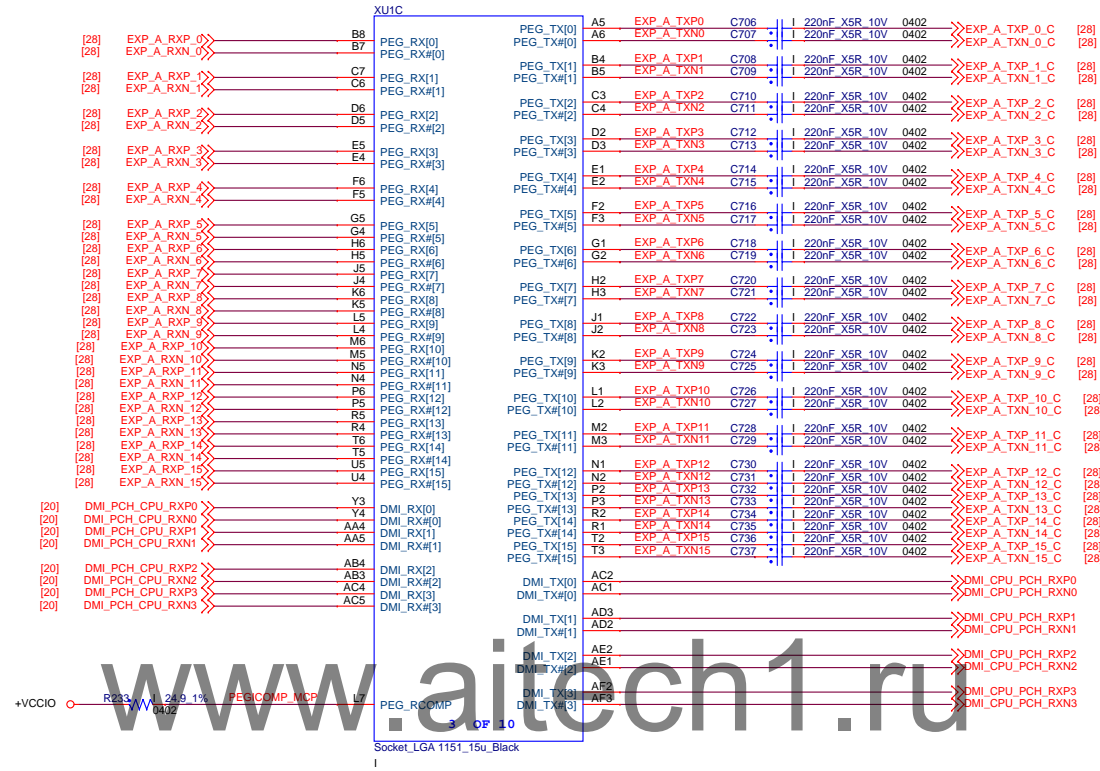
## ALL PINS HAVE INTERNAL PULL-UPS

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG LANE REVERSAL
3			RESERVED
4	DISABLE see table above	ENABLE "0"	eDP enable
5			PEG0CFGSEL[0] x16
6			PEG0CFGSEL[1] x16
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8-19			RESERVED

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# MCP - PCIE,DMI,FDI,DDI

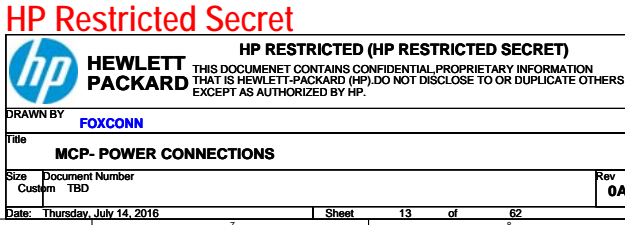


According to intel skylake cpu eds,  
CPU only support three DDI interface display  
at the same time.

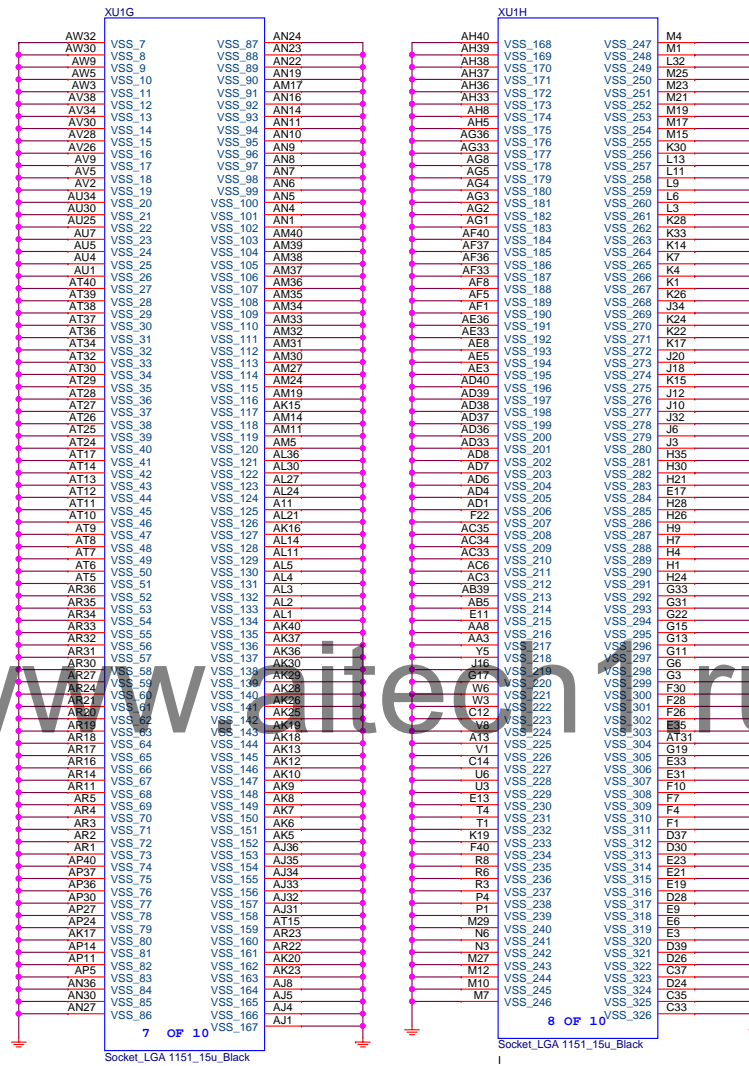
Only Edp lanes[2:3] support DP to VGA  
converter according to Intel skylake EDS.

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Title <b>MCP- PCI/DMI/DDI</b>					
Size	Document Number	Rev			
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Date: Thursday, July 14, 2016		Sheet		17	of 62

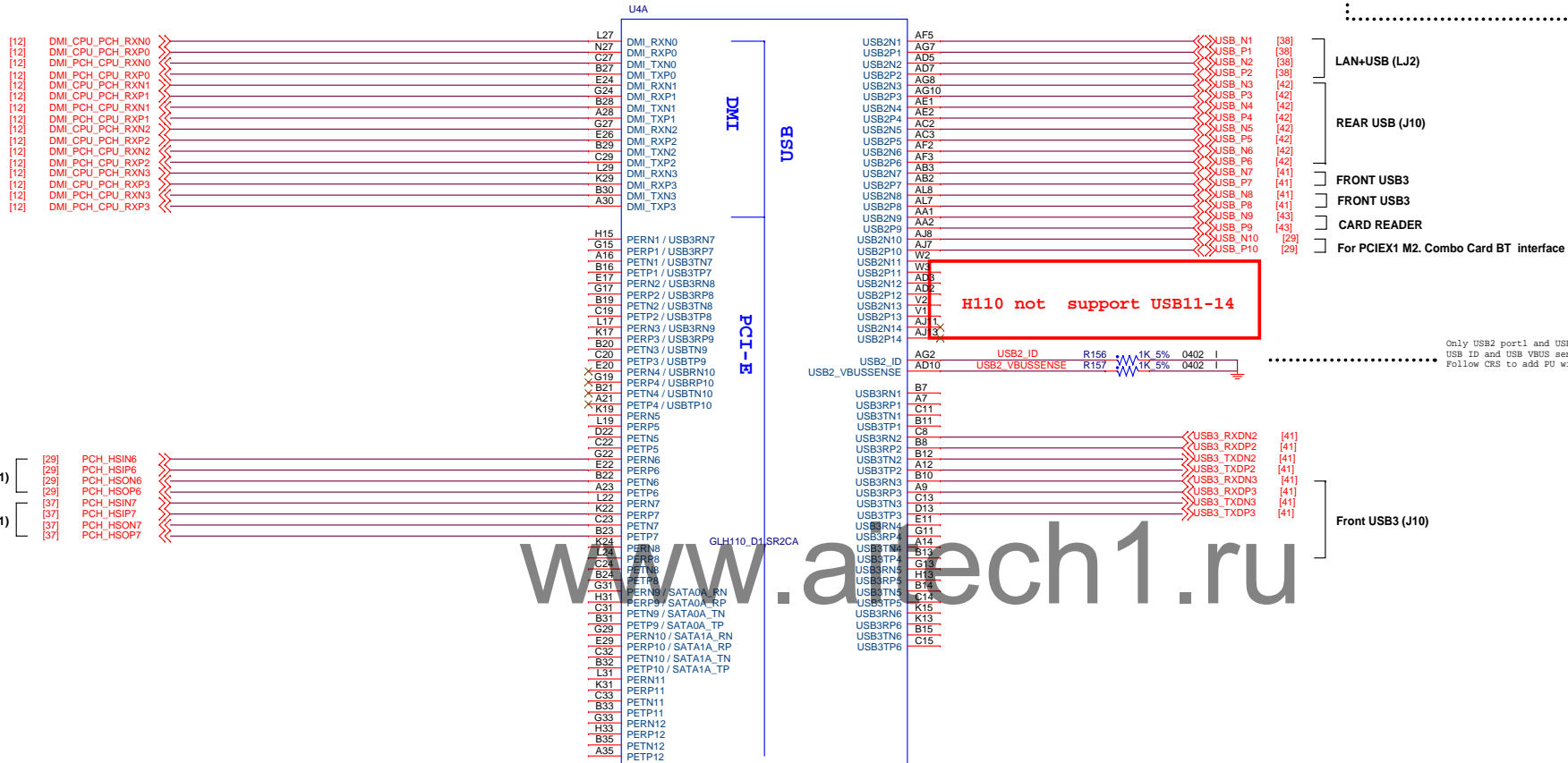


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USB3 and USB2 port mapping is not clear in PDG.  
Have to check again if Intel releases new PDG.




Only USB2 port1 and USB3 Port1 can support On the go function  
USB ID and USB VBUS sense are for OTG function.  
Follow CWS to add PU with lkhcm.

H110 not support USB11-14

Front USB3 (J10)

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Title <b>PCH - DMI/PCI-E/USB2-3</b>					
Size	Document Number				Rev
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[39] SATA\_RXN0  
[39] SATA\_RXP0  
[39] SATA\_TXN0  
[39] SATA\_TXP0  
[39] SATA\_RXN1  
[39] SATA\_RXP1  
[39] SATA\_TXN1  
[39] SATA\_TXP1

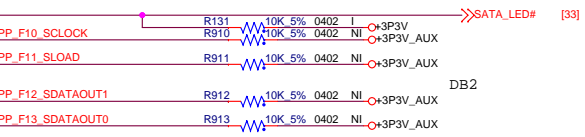


U4B

G36 SATA\_RXN0B / PERN13  
E35 SATA\_RXP0B / PERP13  
C36 SATA\_TXN0B / PETN13  
B36 SATA\_TXP0B / PETP13  
D39 SATA\_RXN1B / PERN14  
E37 SATA\_RXP1B / PERP14  
B38 SATA\_TXN1B / PETN14  
C38 SATA\_TXP1B / PETP14  
F41 SATA\_RXN2 / PERN15  
E41 SATA\_RXP2 / PERP15  
B39 SATA\_TXN2 / PETN15  
A39 SATA\_TXP2 / PETP15  
D43 SATA\_RXN3 / PERN16  
E42 SATA\_RXP3 / PERP16  
A40 SATA\_TXN3 / PETN16  
H42 SATA\_TXP3 / PETP16  
H40 SATA\_RXN4 / PERN17  
E45 SATA\_RXP4 / PERP17  
F45 SATA\_TXN4 / PETN17  
K37 SATA\_TXP4 / PETP17  
G37 SATA\_RXN5 / PERN18  
G45 SATA\_RXP5 / PERN18  
G44 SATA\_TXN5 / PETN18  
L37 SATA\_TXP5 / PERP18  
L39 SATA\_RXN6 / PERN19  
H43 SATA\_RXP6 / PERP19  
H44 SATA\_TXN6 / PETN19  
N38 SATA\_TXP6 / PETP19  
N39 SATA\_RXN7 / PERN20  
K44 SATA\_RXP7 / PERN20  
J45 SATA\_TXN7 / PETN20  
SATA\_TXP7 / PETP20

GPP\_E0\_SATAXPICIE0\_SATAGP0  
GPP\_E1\_SATAXPICIE1\_SATAGP1  
GPP\_E2\_SATAXPICIE2\_SATAGP2  
GPP\_F0\_SATAXPICIE3\_SATAGP3  
GPP\_F1\_SATAXPICIE4\_SATAGP4  
GPP\_F2\_SATAXPICIE5\_SATAGP5  
GPP\_F3\_SATAXPICIE6\_SATAGP6  
GPP\_F4\_SATAXPICIE7\_SATAGP7  
GPP\_E8\_SATALED\_N  
GPP\_F10\_SCLK  
GPP\_F11\_SLOAD  
GPP\_F12\_SDATAOUT1  
GPP\_F13\_SDATAOUT0  
GPP\_F19\_EDP\_VDDEN  
GPP\_F20\_EDP\_BKLTEN  
GPP\_F21\_EDP\_BKLCTL  
GPP\_E3\_CPU\_GP0  
GPP\_E7\_CPU\_GP1  
GPP\_E4\_DEVSLP0  
GPP\_E5\_DEVSLP1  
GPP\_E6\_DEVSLP2  
GPP\_F5\_DEVSLP3  
GPP\_F6\_DEVSLP4  
GPP\_F7\_DEVSLP5  
GPP\_F8\_DEVSLP6  
GPP\_F9\_DEVSLP7  
GPP\_I0\_DDPB\_HPD0  
GPP\_I1\_DDPB\_HPD1  
GPP\_I2\_DDPB\_HPD2  
GPP\_I3\_DDPB\_HPD3  
GPP\_I4\_EDP\_HPD  
GPP\_I5\_DDPB\_CTRLCLK  
GPP\_I6\_DDPB\_CTRLCLK  
GPP\_I7\_DDPB\_CTRLCLK  
GPP\_I8\_DDPB\_CTRLCLK  
GPP\_I9\_DDPB\_CTRLCLK  
GPP\_I10\_DDPB\_CTRLCLK

AG36  
AG35  
AG39  
AD35  
AD31  
AD38  
AC43  
AB44  
AD44  
AB33  
AB35  
AA45  
AA44  
W42  
W35  
W36  
Y44  
W39  
V44  
AD43  
AD42  
AD39  
AC44  
Y43  
Y41  
W44  
W43



Need to check Intel design guide for OC# port mapping

USB2 [1-8] = OC[0-3]  
USB2 [9-14] = OC[4-7]

[27] DDP\_HPD\_R  
[44] DPE\_HPD\_R



VP phase add R965 to support Intel ME/TXE FW Update capability

[21,45] FLASH\_OVERRIDE#



[27] DDPD\_CTRLCLK  
[27] DDPD\_CTRLCLK



AF41  
AE44

AG42  
AG43  
AE45  
AB41  
AB42  
AB43  
AB36  
AB39

AW4  
AY2  
AV4  
BA4  
BD7  
BA5  
BC4  
BB3  
BD6  
BE5  
BE6

GLH110.D1.SR2CA

U4F

GPP\_A0\_RCIN\_N\_ESPI\_ALERT1\_N  
GPP\_A1\_LAD0\_ESPI\_IO0  
GPP\_A2\_LAD1\_ESPI\_IO1  
GPP\_A3\_LAD2\_ESPI\_IO2  
GPP\_A4\_LAD3\_ESPI\_IO3  
GPP\_A5\_LFRAME\_N\_ESPI\_CS0\_N  
GPP\_A6\_SERIRQ\_ESPI\_CS1\_N  
GPP\_A7\_PIRQA\_N\_ESPI\_ALERT0\_N  
GPP\_A8\_CLKRUN\_N  
GPP\_A9\_CLKOUT\_LPC0\_ESPI\_CLK  
GPP\_A10\_CLKOUT\_LPC1  
GPP\_A11\_PME\_N  
GPP\_A12\_BMBUSY\_N\_ISH\_GP6\_SX\_EXIT\_HOLDOFF\_N  
GPP\_A13\_SUSWARN\_N\_SUSPWDNACK  
GPP\_A14\_SUS\_STAT\_N\_ESPI\_RESET\_N  
GPP\_A15\_SUSACK\_N  
GPP\_A16\_CLKOUT\_48  
GPP\_A17\_ISH\_GP7  
GPP\_A18\_ISH\_GP0  
GPP\_A19\_ISH\_GP1  
GPP\_A20\_ISH\_GP2  
GPP\_A21\_ISH\_GP3  
GPP\_A22\_ISH\_GP4  
GPP\_A23\_ISH\_GP5

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[30] SIO\_KBRST#  
[34] LPC\_AD0  
[34] LPC\_AD1  
[34] LPC\_AD2  
[34] LPC\_AD3  
[34] LPC\_FRAME#  
[30,34] SER\_IRQ



GLH110.D1.SR2CA

U4F

GPP\_G0\_FAN\_TACH\_0  
GPP\_G1\_FAN\_TACH\_1  
GPP\_G2\_FAN\_TACH\_2  
GPP\_G3\_FAN\_TACH\_3  
GPP\_G4\_FAN\_TACH\_4  
GPP\_G5\_FAN\_TACH\_5  
GPP\_G6\_FAN\_TACH\_6  
GPP\_G7\_FAN\_TACH\_7  
GPP\_G8\_FAN\_PWM\_0  
GPP\_G9\_FAN\_PWM\_1  
GPP\_G10\_FAN\_PWM\_2  
GPP\_G11\_FAN\_PWM\_3  
GPP\_G12\_GSXDOUT  
GPP\_G13\_GSXSLOAD  
GPP\_G14\_GSXDIN  
GPP\_G15\_GSXSRESET\_N  
GPP\_G16\_GSXCCLK  
GPP\_G17\_ADR\_COMPLETE  
GPP\_G18\_NMI\_N  
GPP\_G19\_SMI\_N  
GPP\_G20  
GPP\_G21  
GPP\_G22  
GPP\_G23  
SPI0\_CLK  
SPI0\_CS#  
SPI0\_CS1#  
SPI0\_IO2  
SPI0\_IO3  
SPI0\_MISO  
SPI0\_MOSI  
SPI0\_CS2#  
PM\_DOWN  
PM\_SYNC  
PECI

6 OF 10

GLH110.D1.SR2CA

U43  
U42  
U41  
M44  
U36  
P44  
T45  
T44  
R44  
R43  
U39  
N42  
R36  
R42  
R41  
P43  
N44  
N43  
M45  
R35  
L44  
L43

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

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GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

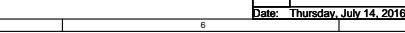
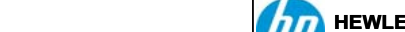
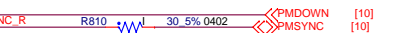
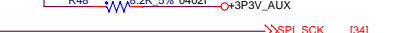
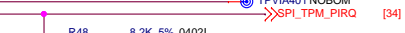
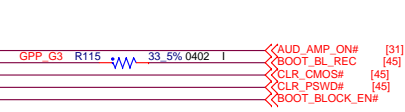
GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3

GPP\_G3



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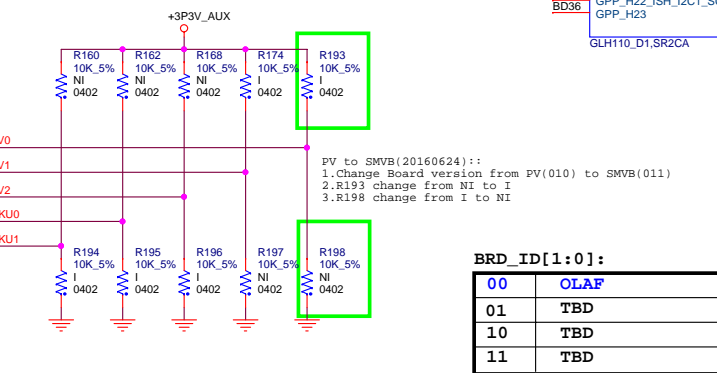
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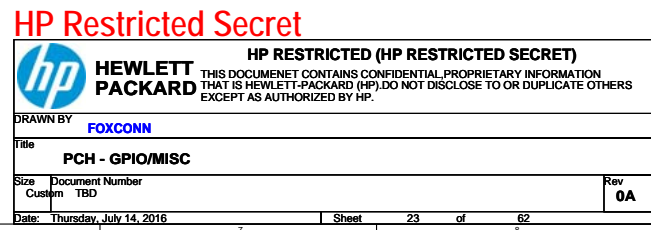
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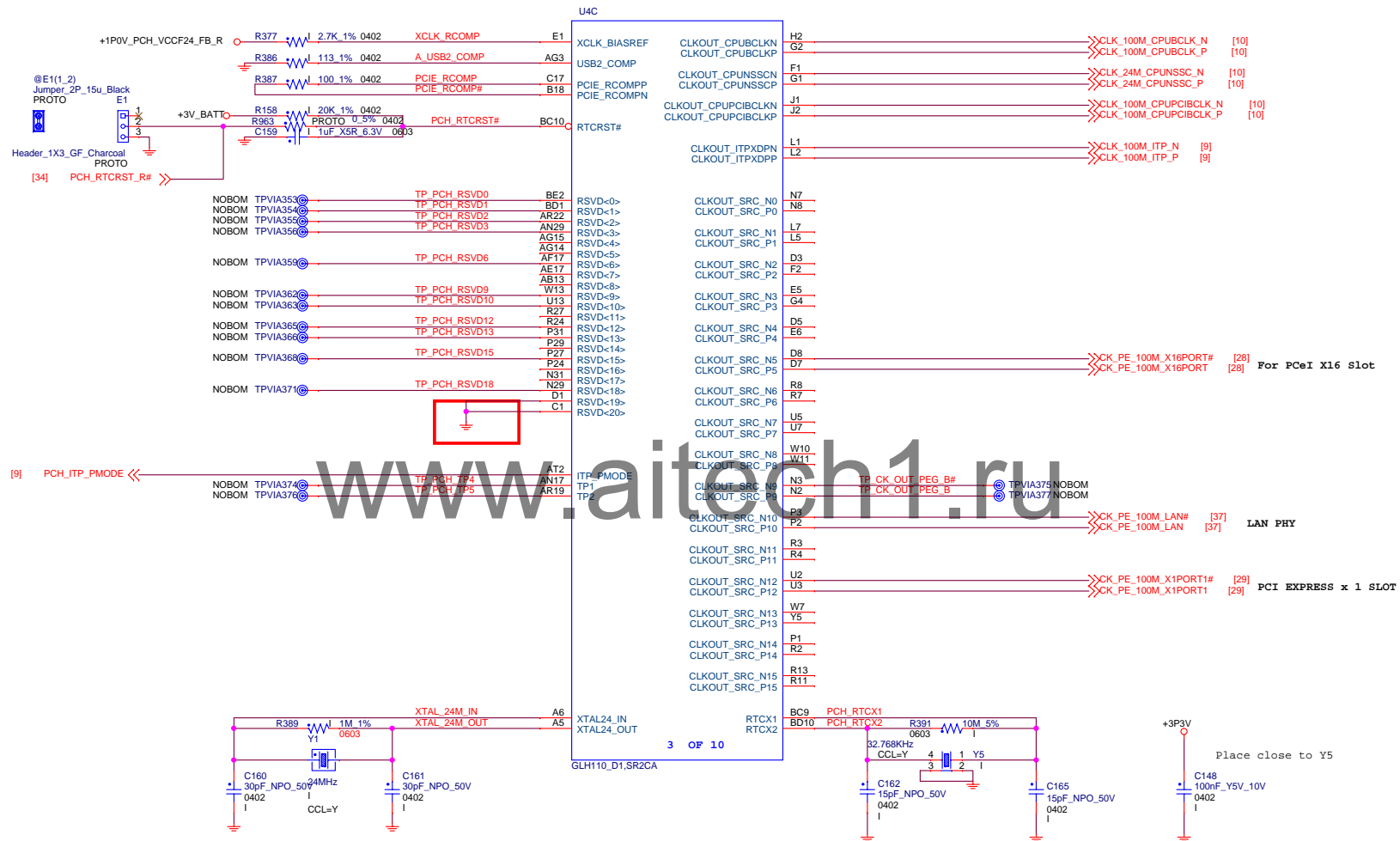


BRD_ID[1:0]:	
00	OLAF
01	TBD
10	TBD
11	TBD

BRD_REV[2:0]:	
000	DB
001	SI
010	PV
011	1.00 (SMVB)
100	1.10 (ECN1)
101	1.20 (ECN2)
110	1.30 (ECN3)
111	1.40 (ECN4)



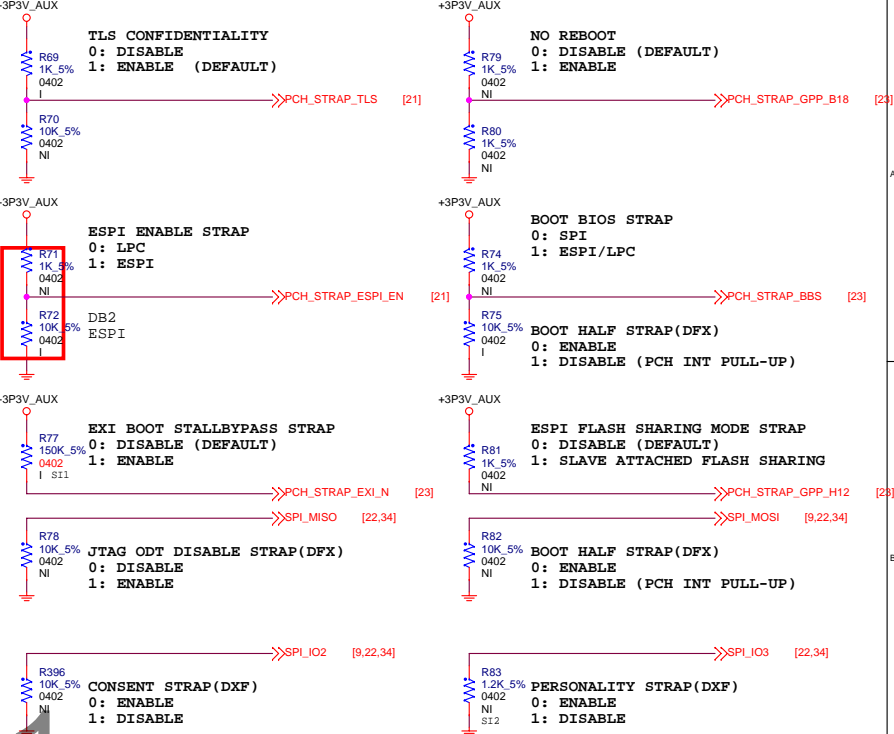
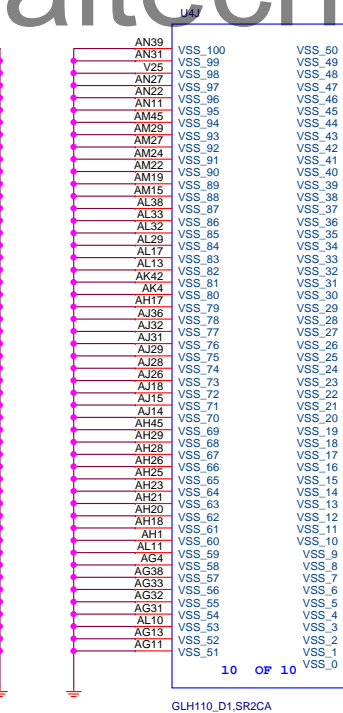
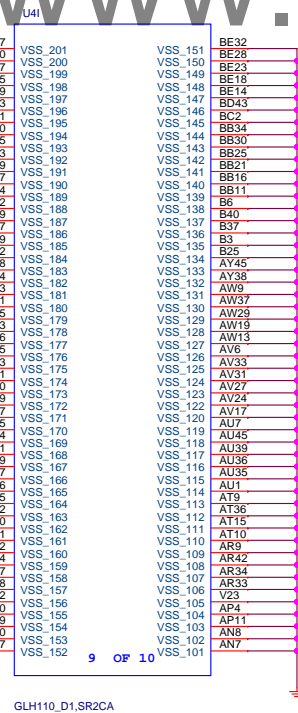
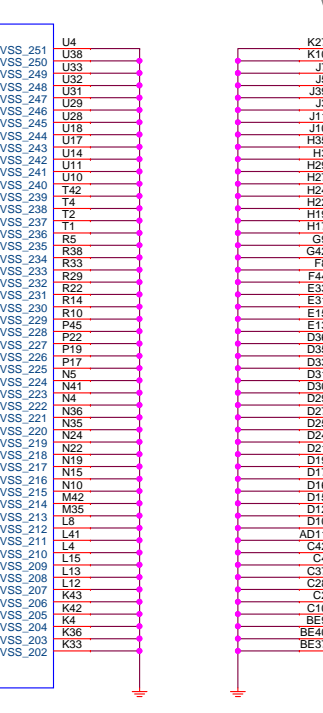
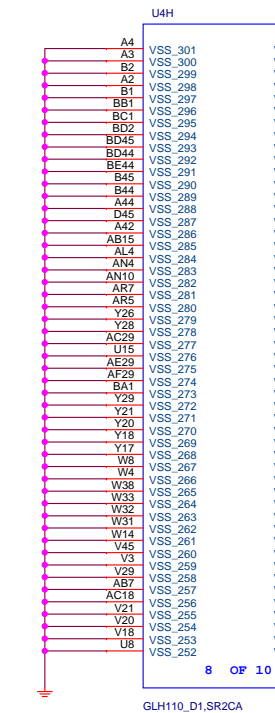
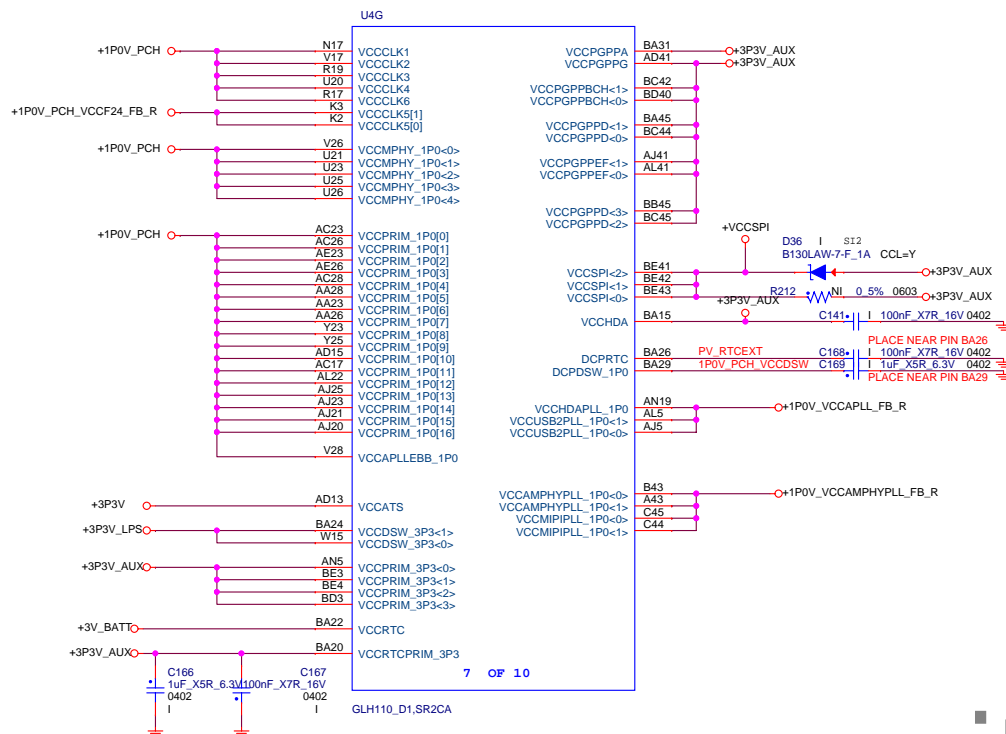
# PCH - CLOCK DISTRIBUTION



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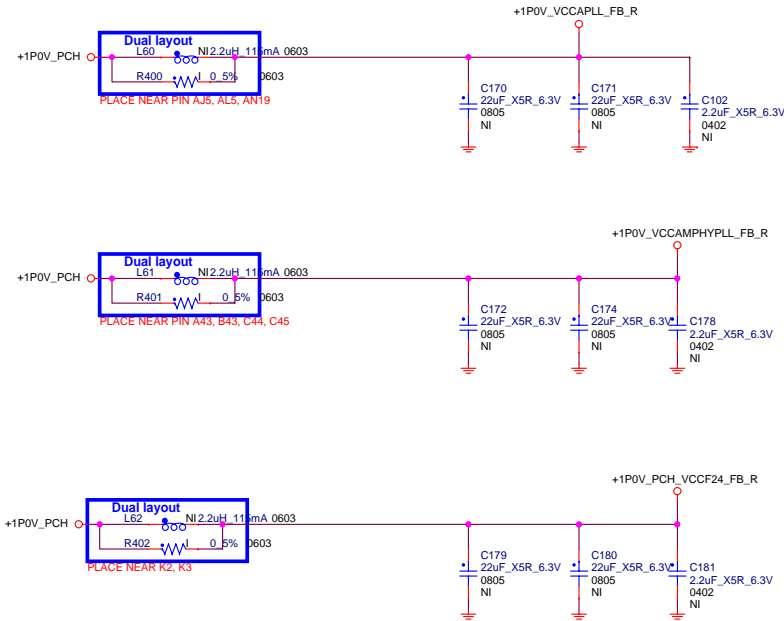
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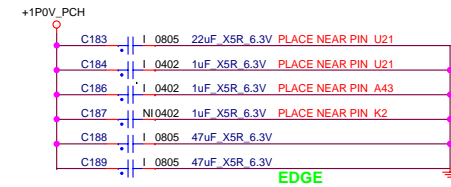
Rev: 0A

SKYLAKE Decoupling & filter

FILTER



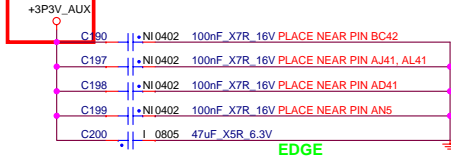
V1.0A



V3.3 DSW



V1.8A / V3.3A



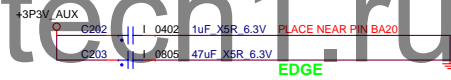
VccPGPPA



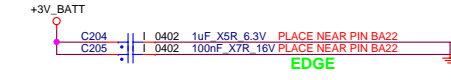
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC



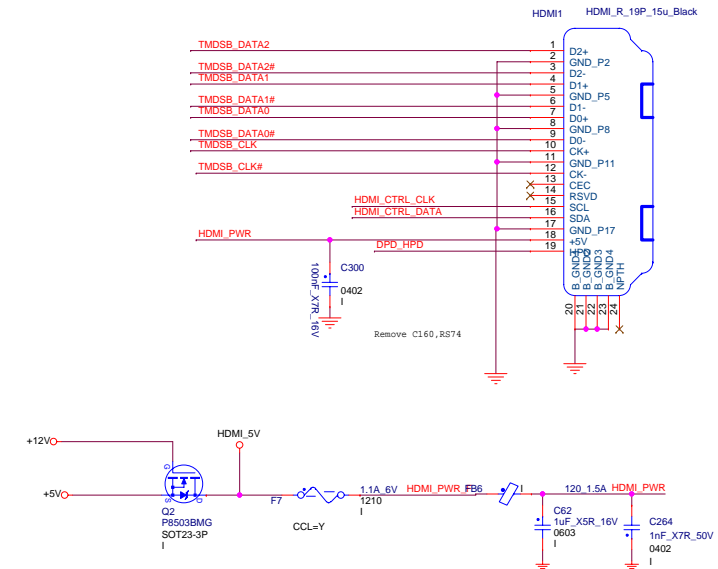
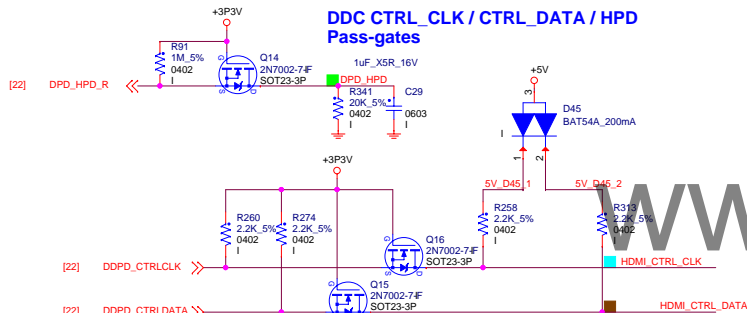
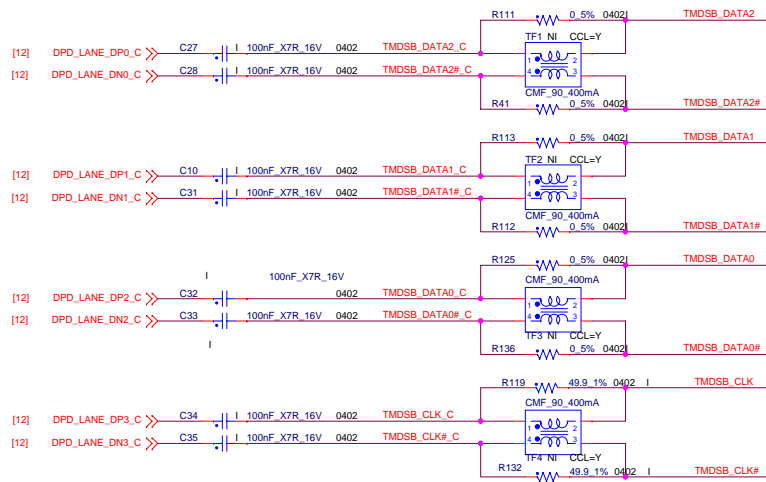
Power Plane Isolation

Need to update for SLK

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

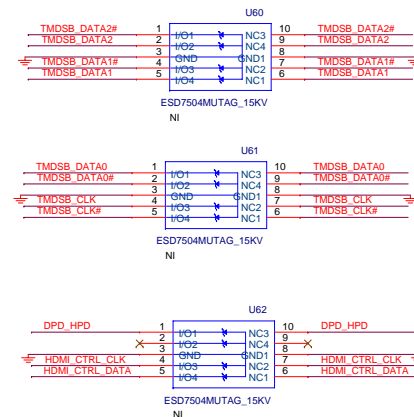
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DRAWN BY <b>FOXCONN</b>					
Title <b>PCH-PLL FILTER &amp; DECOUPLING</b>					
Size	Document Number				Rev
Custom	TBD				0A
Date: Thursday, July 14, 2016		Sheet	26	of	62

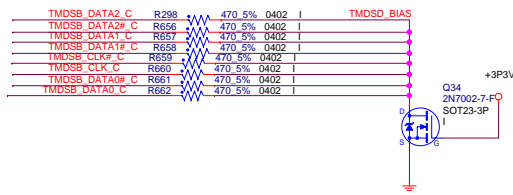


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ESD suppressor



## Cost Reduced Level Shifter Solution



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Title: **HDMI**

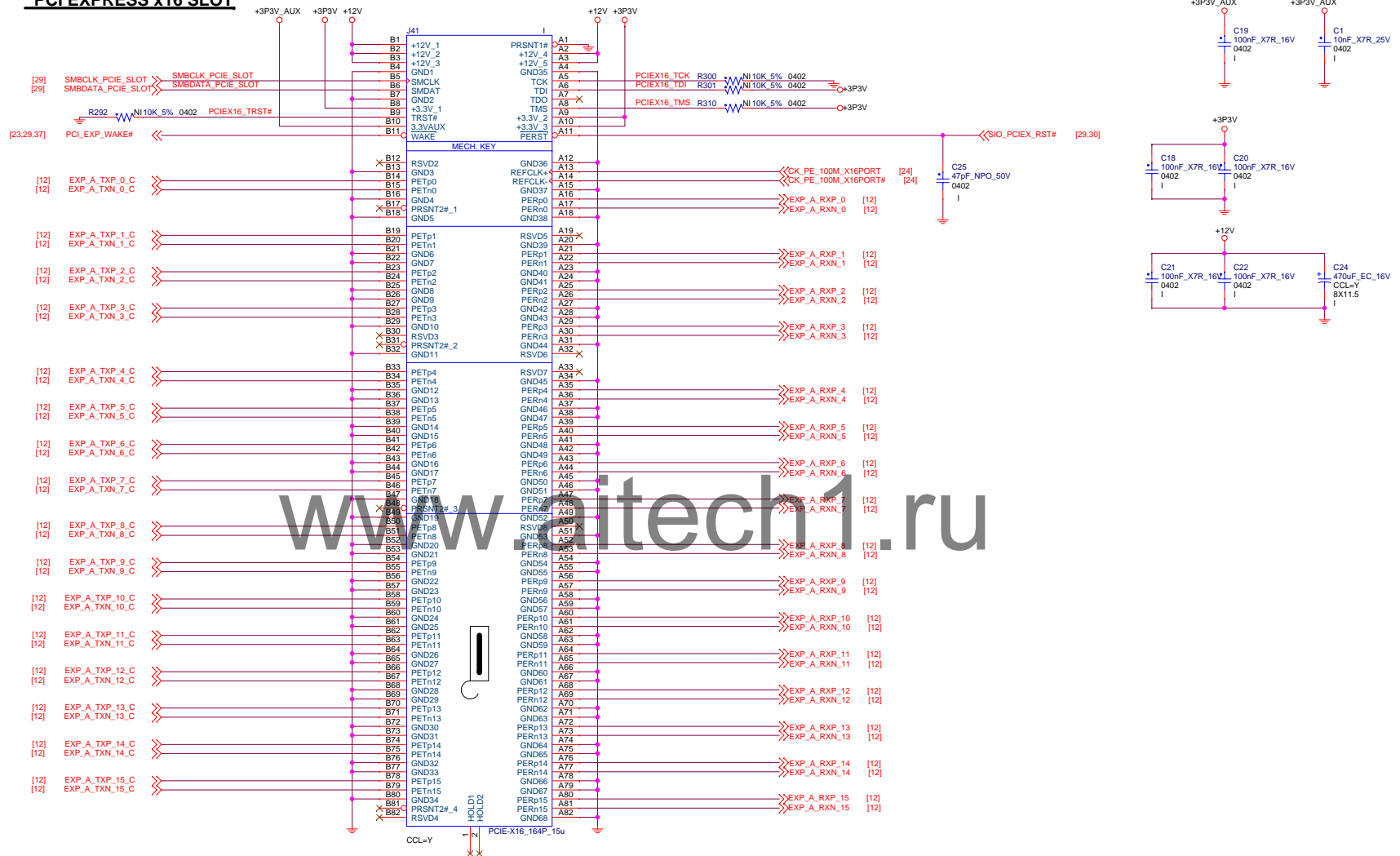
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Custom: TBD

Date: Thursday, July 14, 2016

Sheet: 27 of 62

Rev: **0A**

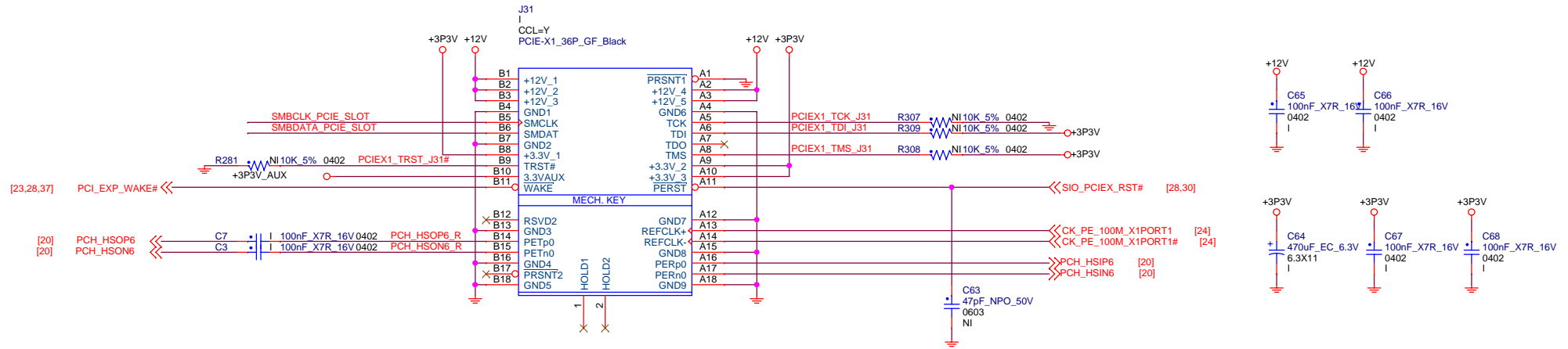
# PCI EXPRESS x16 SLOT



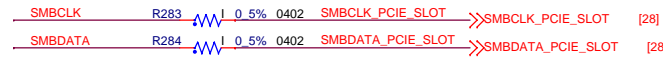
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DRAWN BY <b>FOXCONN</b>			
Title <b>PCIEx16</b>			
Size	Document Number	Rev	
Custom	TBD	0A	
Date:	Thursday, July 14, 2016	Sheet	28 of 62

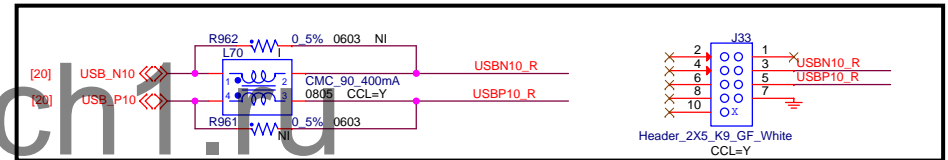
## PCI EXPRESS X1 SLOT1



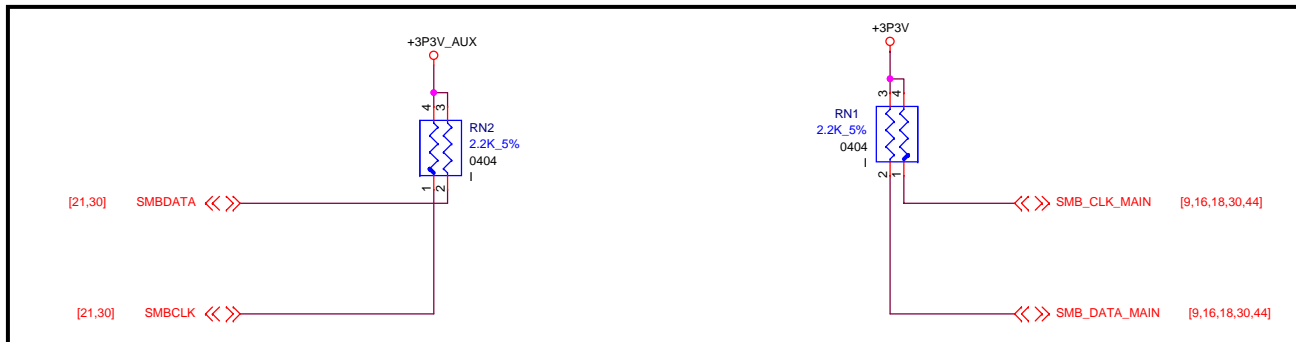
For Monotonic improve use



USB Header for BT Caddy Card.



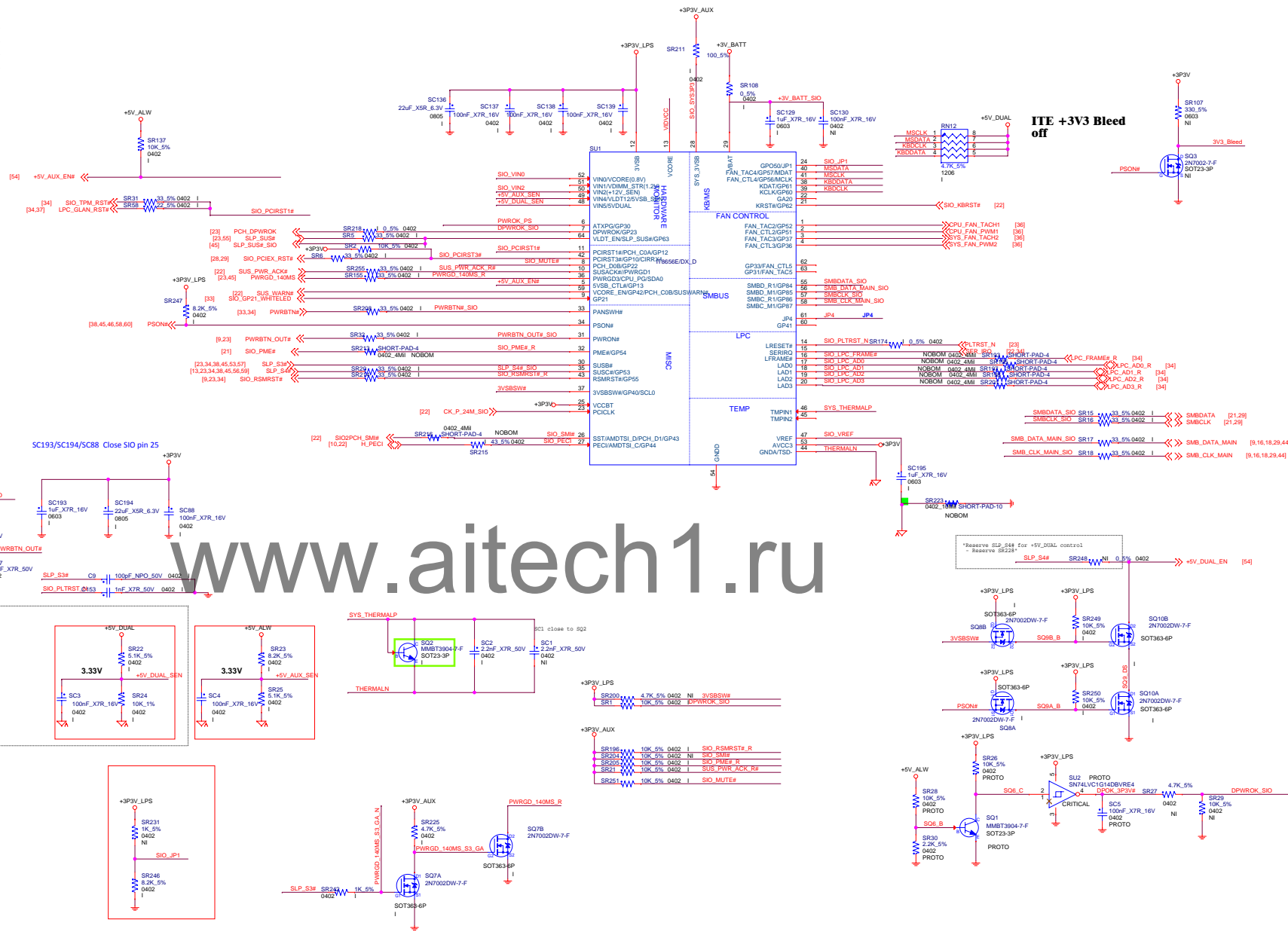
SMBUS Pull High



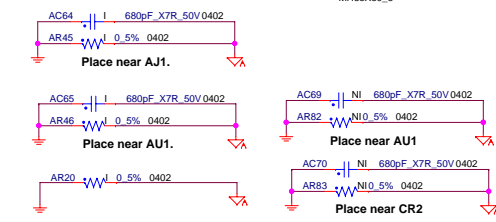
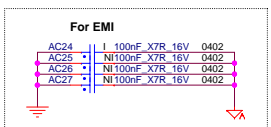
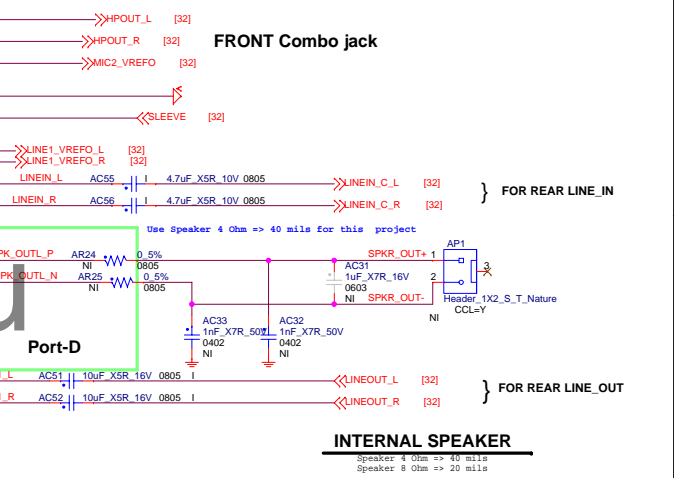
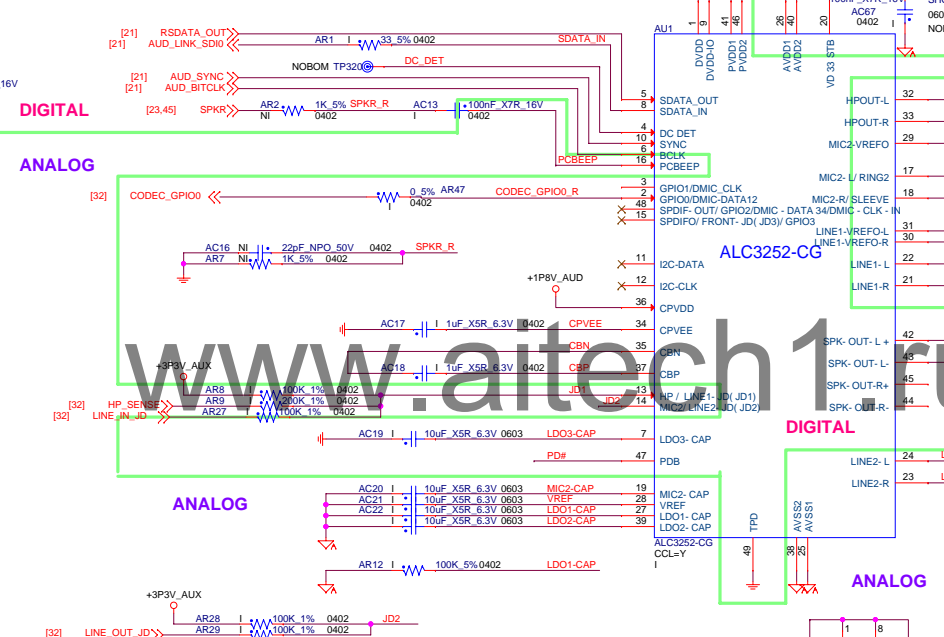
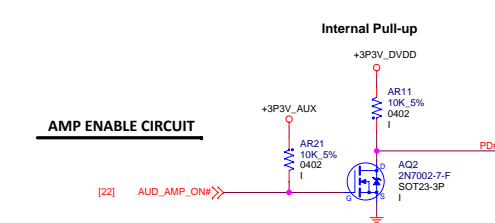
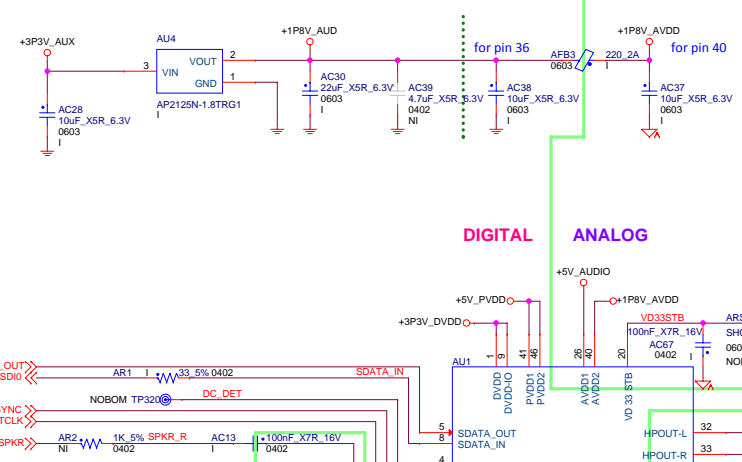
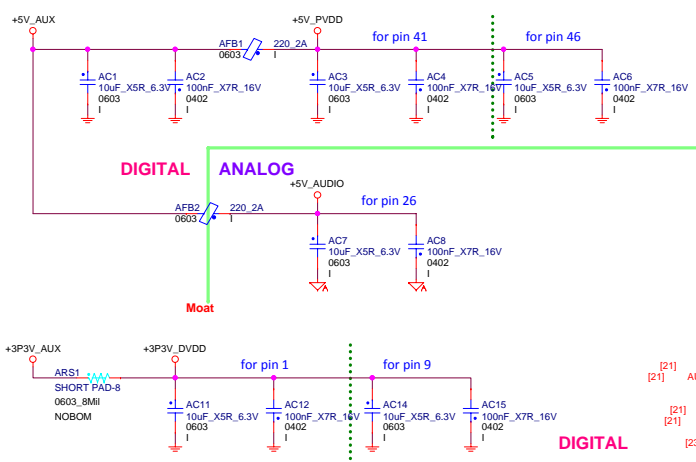
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	Symbol	Value	Description
JP1 Pin-24	DSW_EUP_SEL	1	EUP
		0	DSW
JP4 Pin-61	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence



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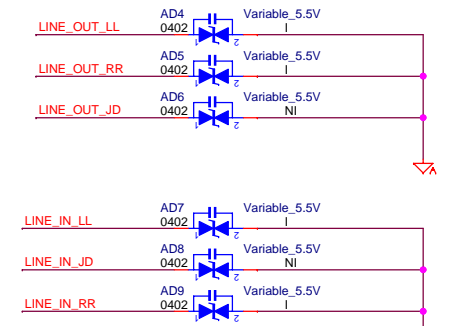
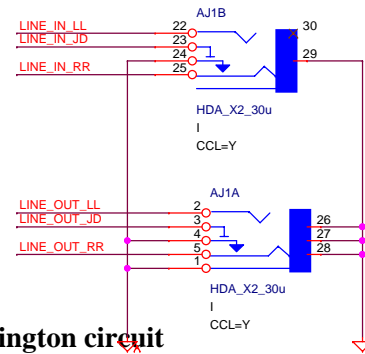
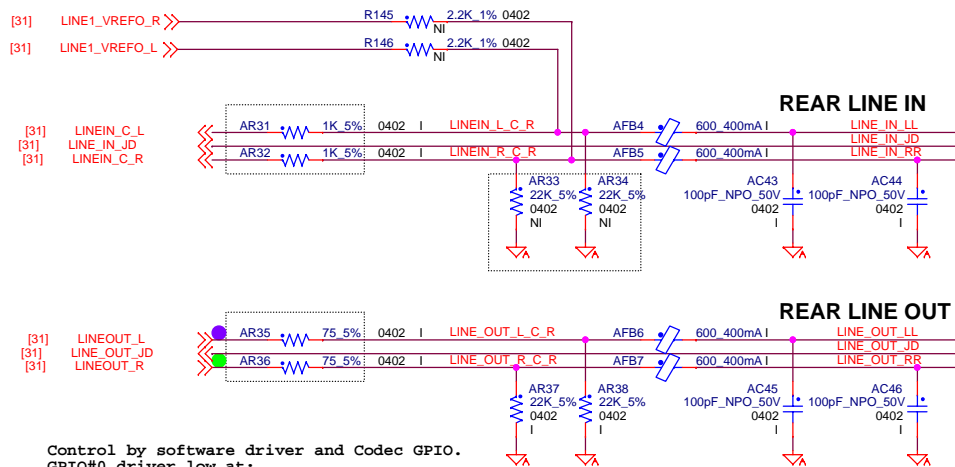
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File **AUDIO ALC3252**

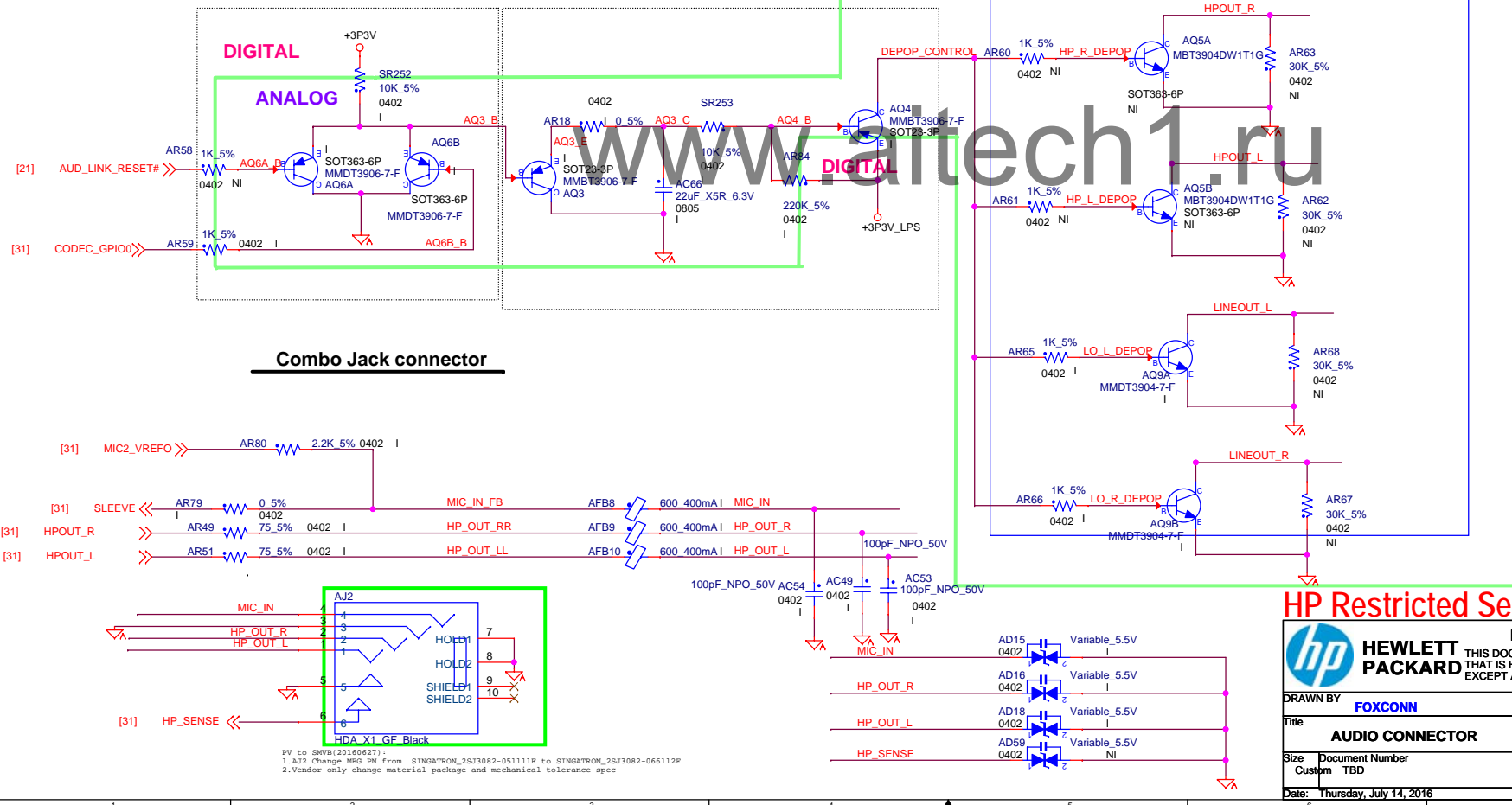
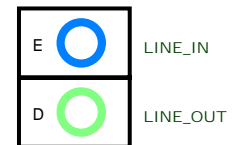
Size Document Number Custom TBD

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## Audio Jack



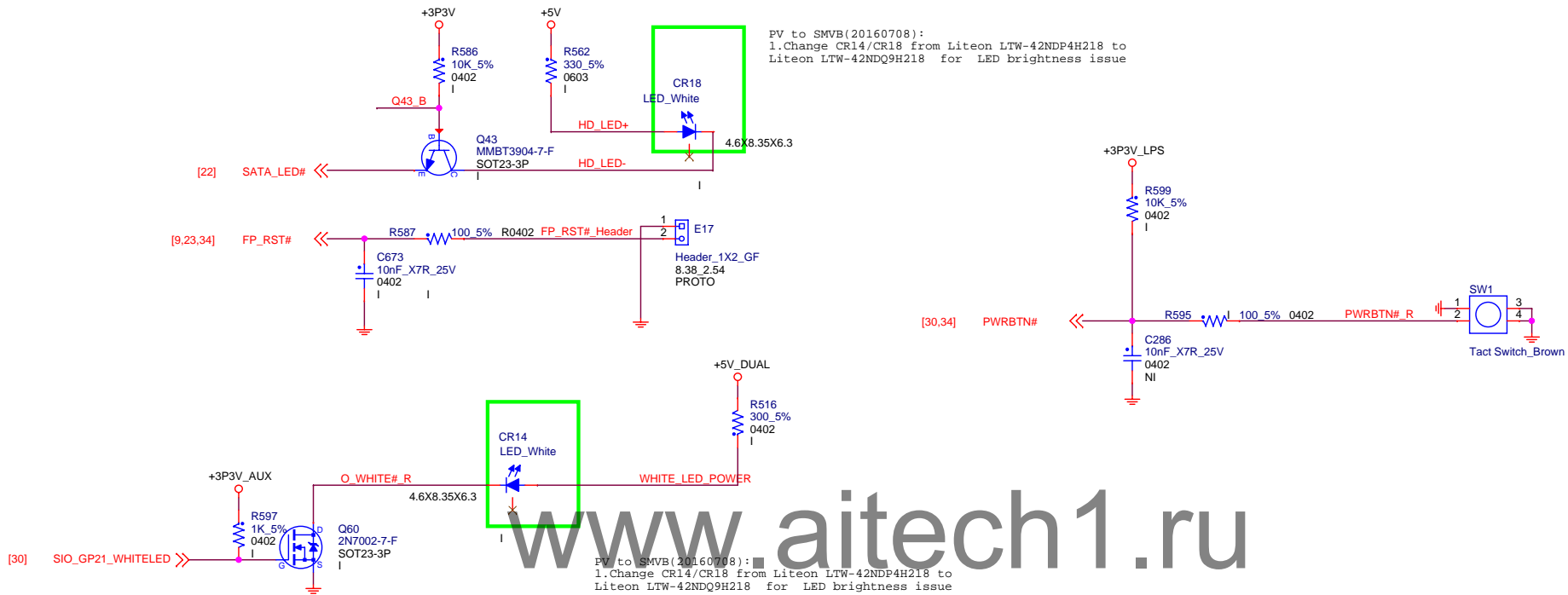
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Title <b>AUDIO CONNECTOR</b>					
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Custom	TBD	0A			
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## Front Panel

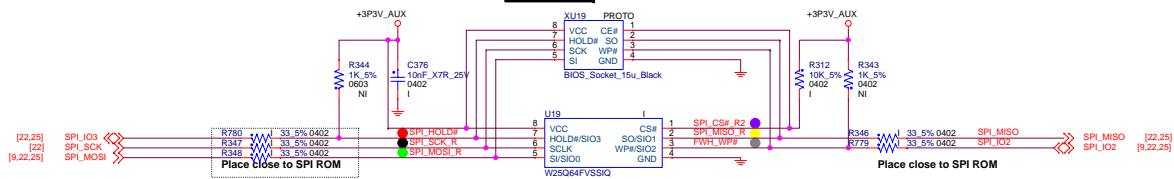
PV to SMVB(20160708):  
1.Change CR14/CR18 from Liteon LTW-42NDP4H218 to  
Liteon LTW-42NDQ9H218 for LED brightness issue



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Title <b>FRONT PANEL</b>			
Size <b>B</b>	Document Number <b>TBD</b>		Rev <b>0A</b>
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## SPI ROM

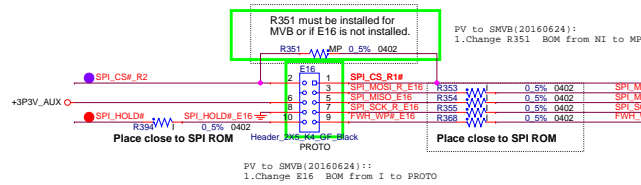


## SPI ROM RECOVERY HEADER/JUMPER

The header traces should be daisy-chain through the header with no stubs.

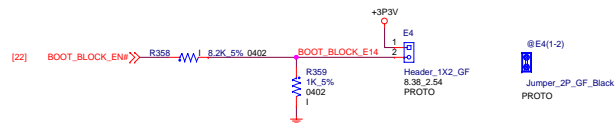
PV to SMVB(20160624)::  
1.Change @E16(1-2) BOM from I to PROTO

@E16(1-2)  
Jumper\_2P\_GF\_Blue  
PROTO  
Place Jumper on Pins 1 and 2



Place close to SPI ROM  
R352 33.5% 0402

## SPI ROM BOOTBLOCK HEADER



## TPM/LPC

For SLB9670 TPM SPI signal

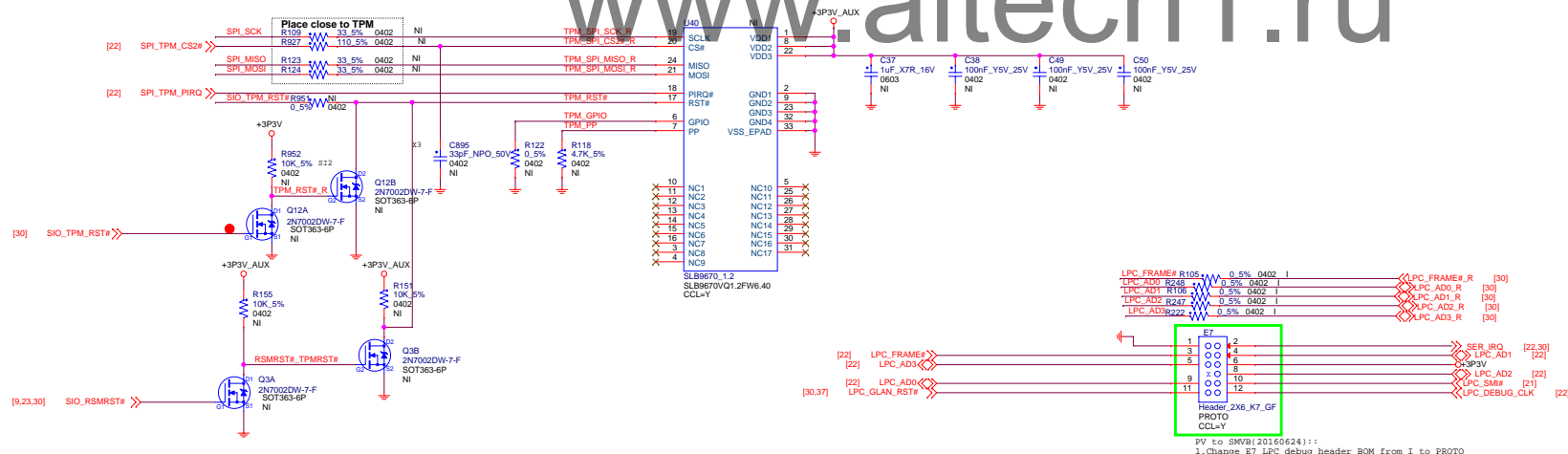
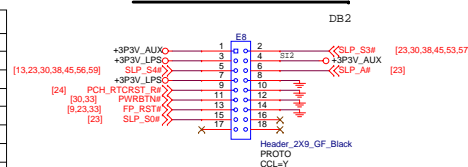


Table 27-4. Pin Location for Dual-in-Line header

Signal Name	Pin		Pin	Signal Name
VccSus3_3	1	o	2	SLP_S3#
VccDSW3_3	3	o	4	SLP_S5#
SLP_S4#	5	o	6	SLP_A#
VccDSW3_3	7	o	8	GND
RTCRST#	9	o	10	GND (for RTCRST#)
PWRBRTN#	11	o	12	GND (for PWRBRTN#)
SYS_RESET#	13	o	14	GND (for SYS_RESET#)
SLP_S0#	15	o	16	NC
NC	17	o	18	NC

## METS/APS TEST HEADER



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File **SPI ROM & LPC DEBUG**


Size Document Number **TBD**

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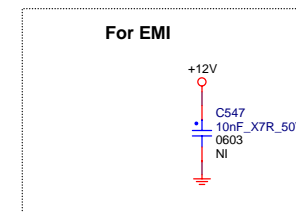
Rev **0A**

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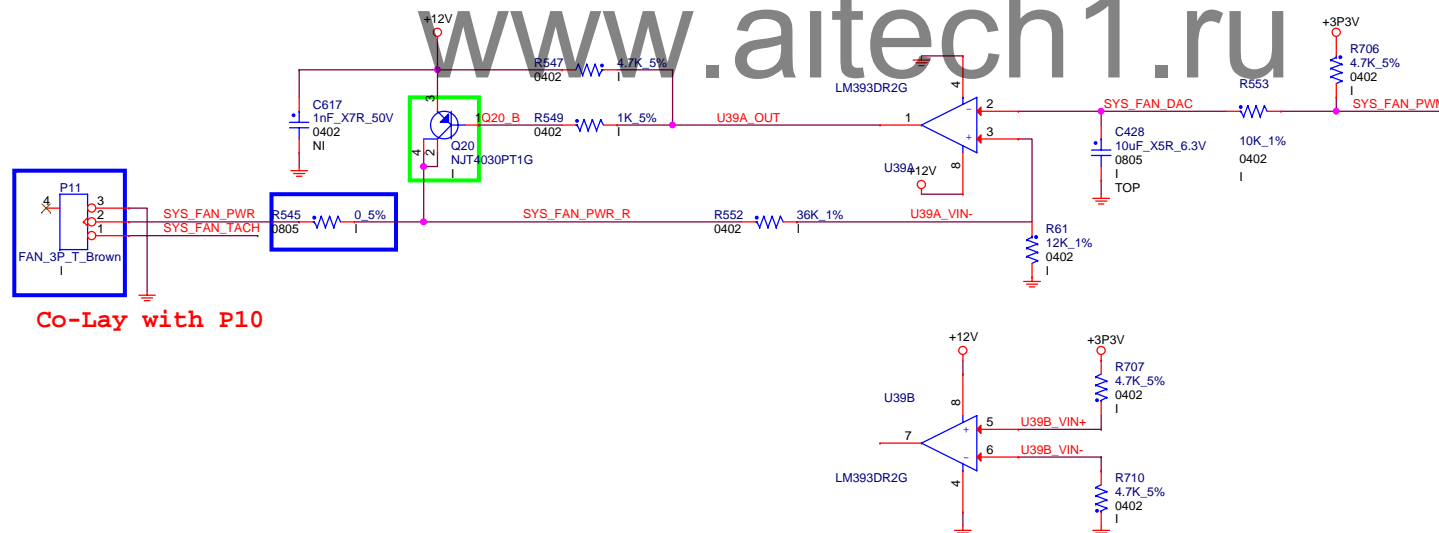
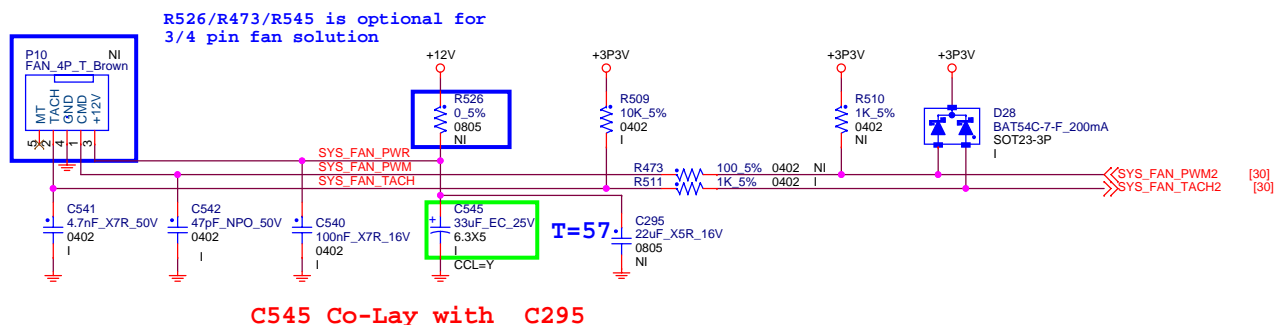
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**Color:** White



**Color: Brown**



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## FAN HEADERS

Size

Document Number

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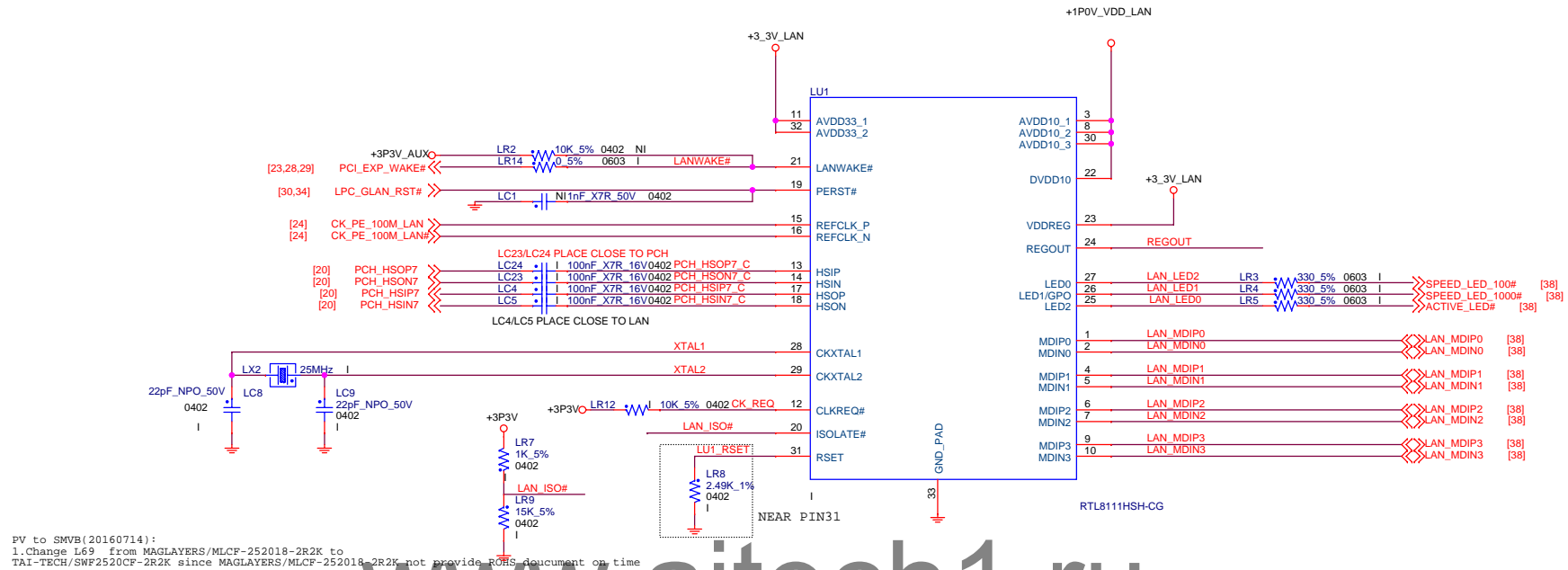
Date: Thursday, July 14, 2016

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Rev	0A
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QA

## Realtek RTL8111HSH-CG



**L69 NEAR PIN24 WITHIN 200MIL**

Wider than 60mil

REGOUT

L69 2.2uH 775mA 1008

Wider than 60mil

LC36 4.7uF\_X5R\_6.3V 0603

LC15 100nF\_X7R\_1 0402

**LC36/LC15 near L69 WITHIN 200MIL**

For 8111HSH Close pin22

For 8111HSH Close pin (8,22,30, 3)

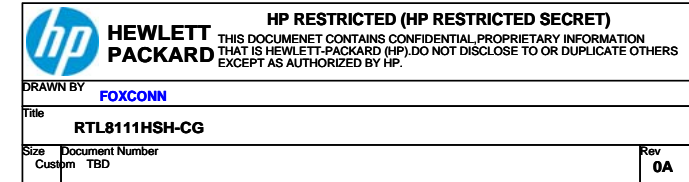
LC2/LC35 near pin 23 WITHIN 200MIL  
To pin23 trace Wider than 40mil

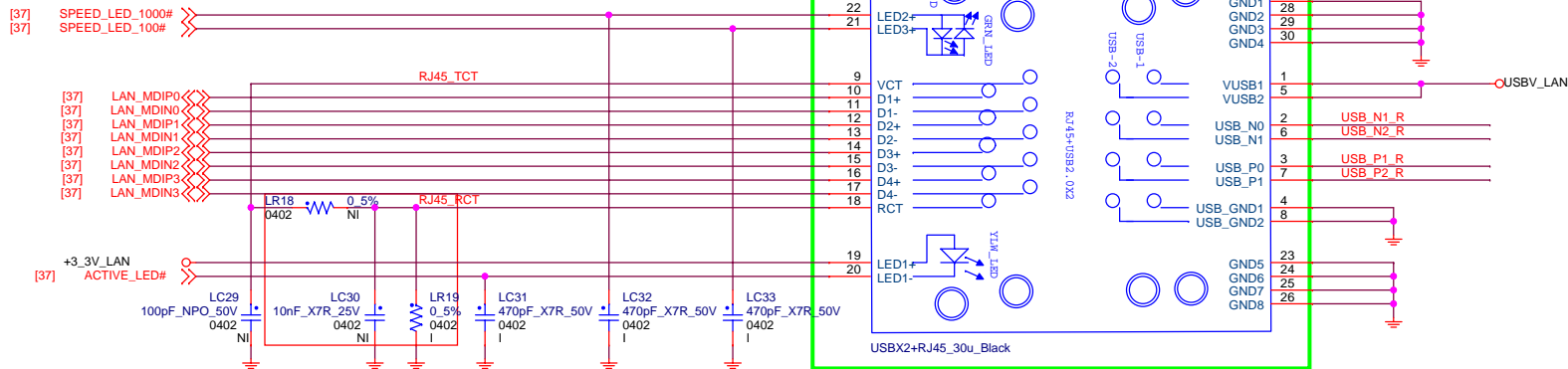
LC2 LC35 Close to VDD33 pin23  
LC6 LC7 Close to VDD33 pin (pin11,32)  
LC20 LC19Close to VDD33 pin (pin11,32)

**EMI Cap**

+3\_3V\_LAN LC34+ 100nF X7R 16V 0402 I

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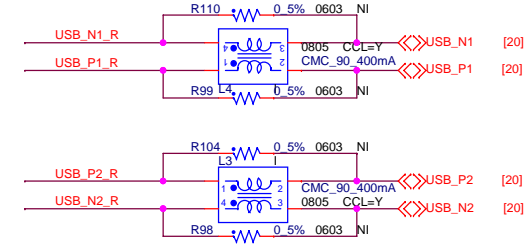




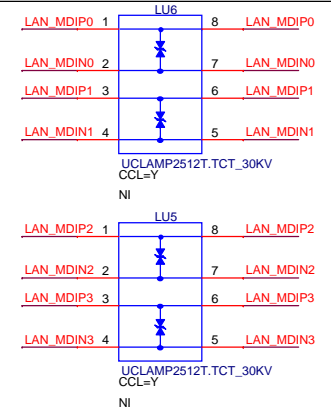
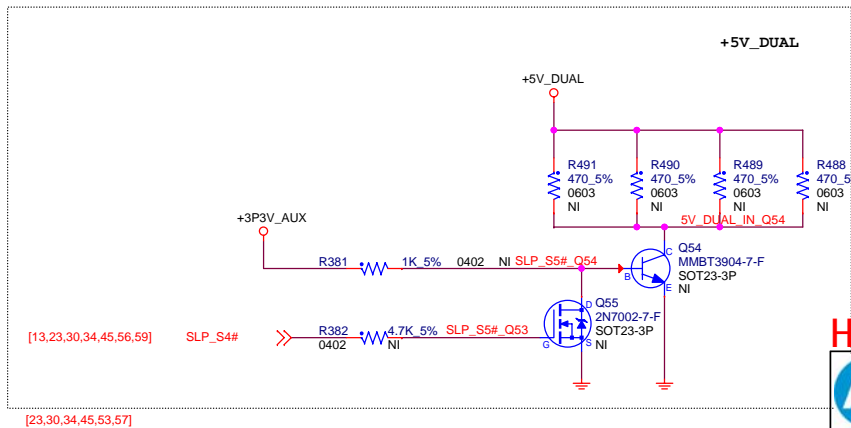
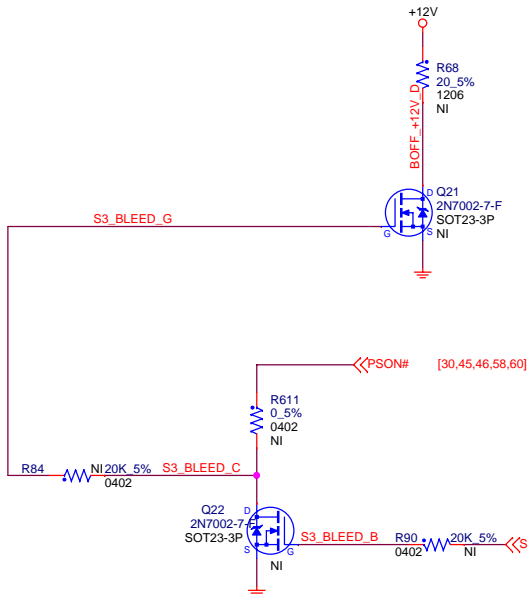
LR19 NI since pin18 has internally connect to GND

10/100M : LC30, LR18==> I, LR19 ==> NI  
1000M : LC30, LR18 ==> NI, LR19 ==> I

PV to SMVB(20160711):  
1.Change LJ2 from FOXCONN\_JFM38U1G-FPV2-4F to  
SPEEDTECH\_RUA2JA-4JR3-BE0-0H for RJ45 offset issue



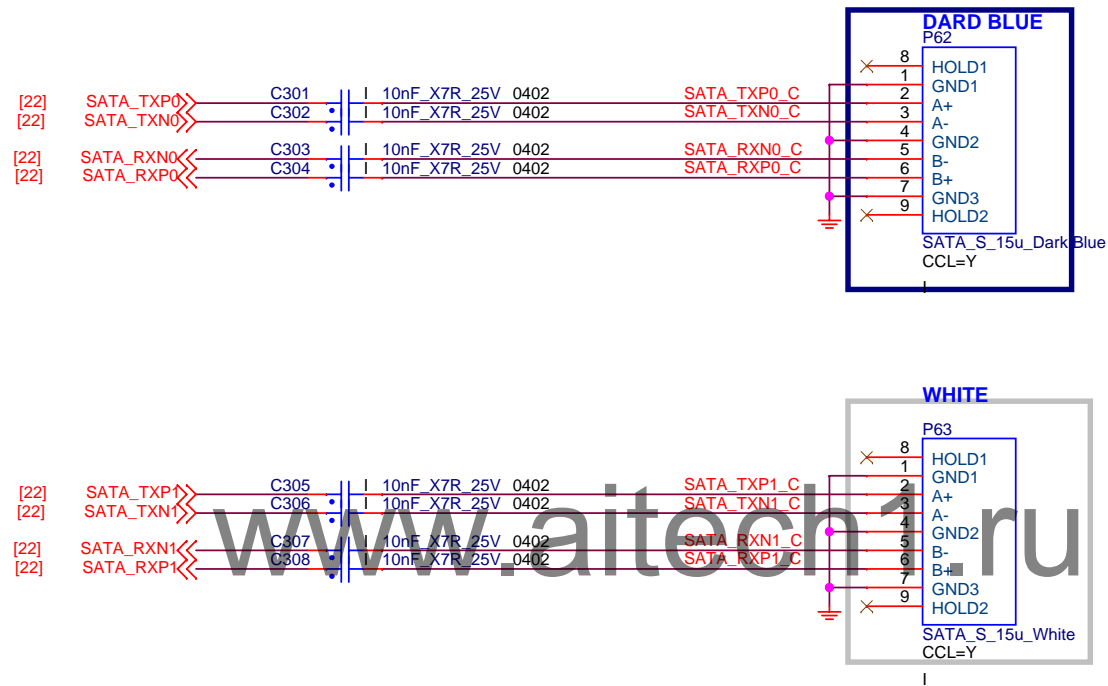
## BLEED-OFF CIRCUITS




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Title <b>RJ45/BLEED OFF/USB X2</b>			
Size <b>Custom</b>	Document Number <b>TBD</b>	Rev <b>0A</b>	
Date: <b>Thursday, July 14, 2016</b>		Sheet <b>38</b>	of <b>62</b>

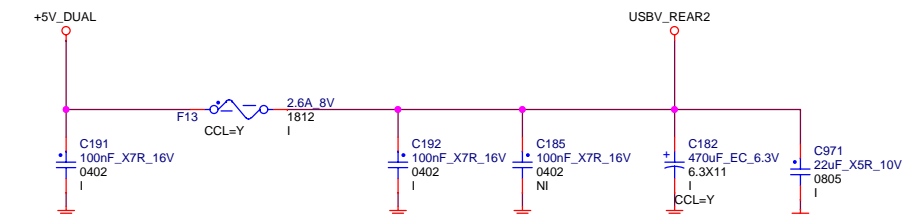
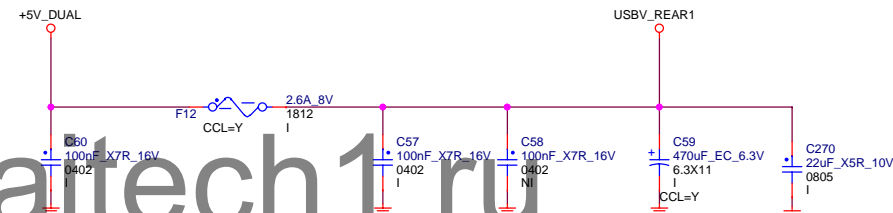
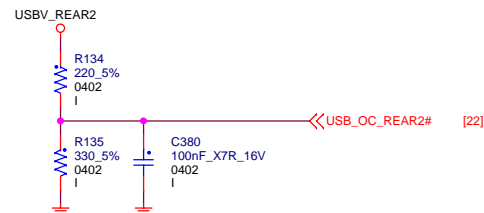
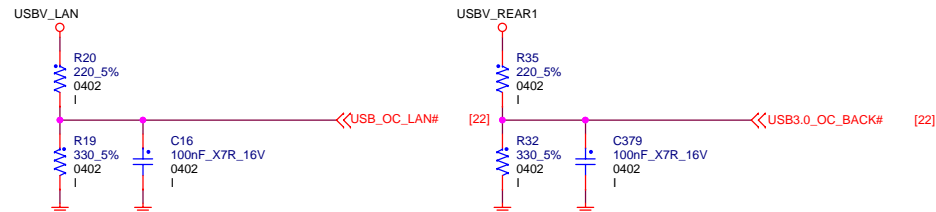
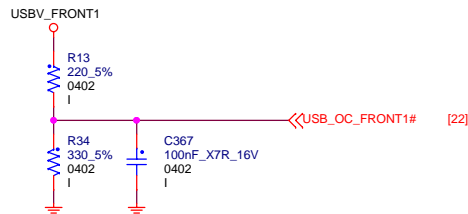
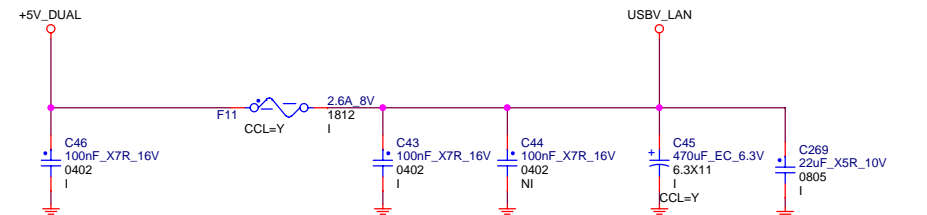
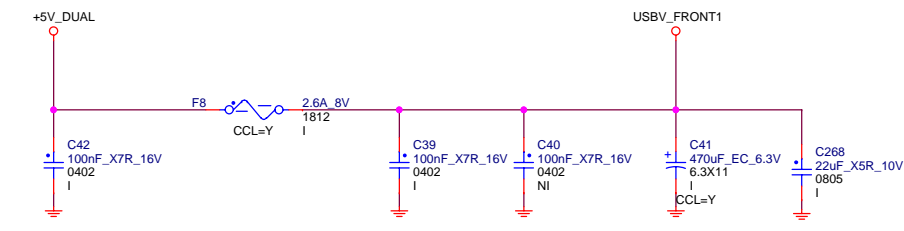
## SATA 3.0 Port0,1




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Custom	TBD				<b>0A</b>
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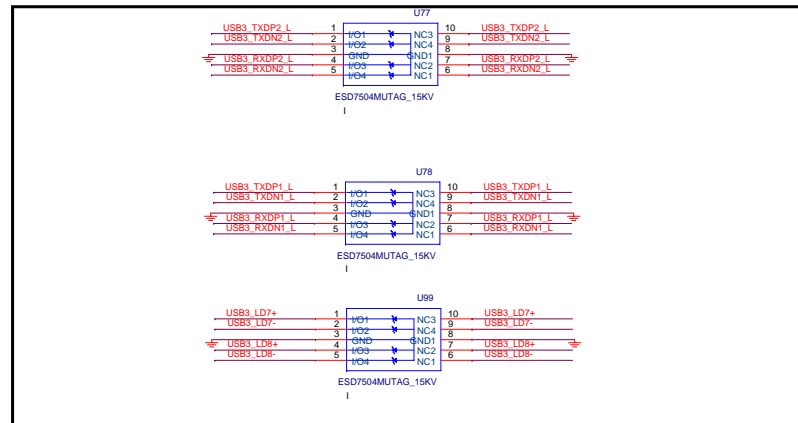
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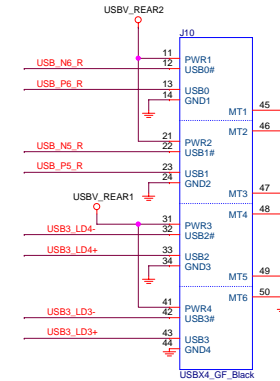
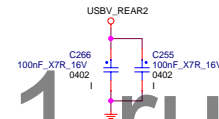
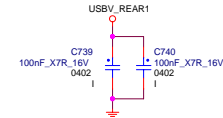
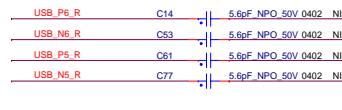
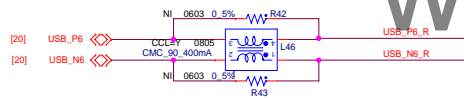
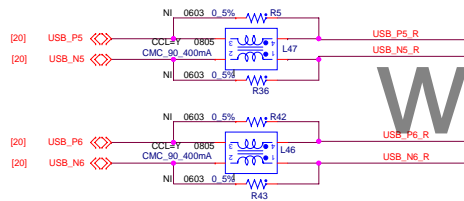
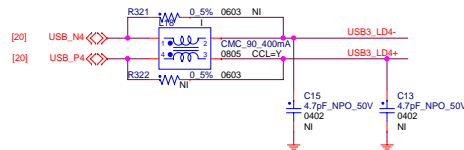
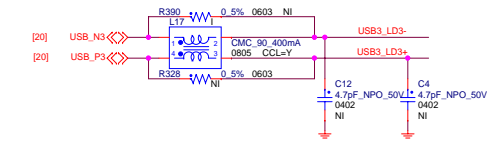
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Title <b>USB POWER</b>					
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Custom	TBD				<b>0A</b>
Date:	Thursday, July 14, 2016	Sheet	40	of	62



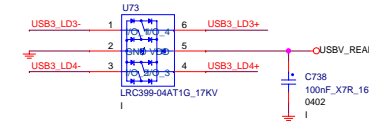
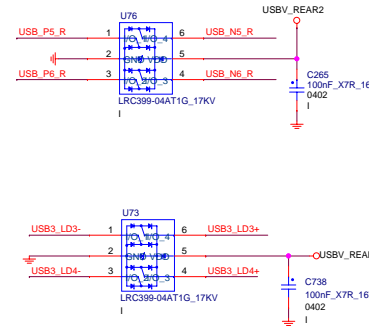


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File	<b>FRONT USB3.0 X2</b>		
Size	Document Number	Rev	
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# REAR USB2.0X4

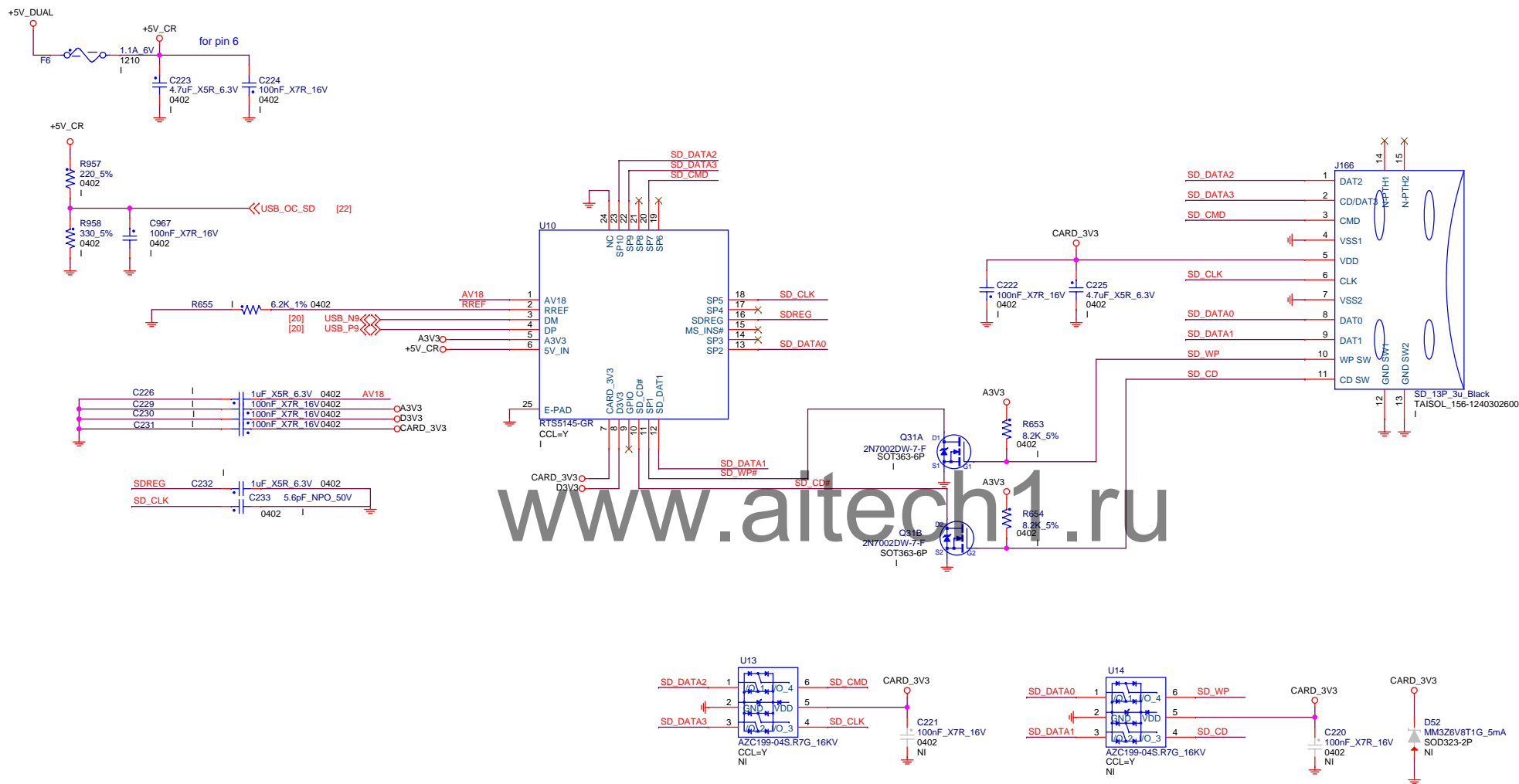


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ESD suppressor




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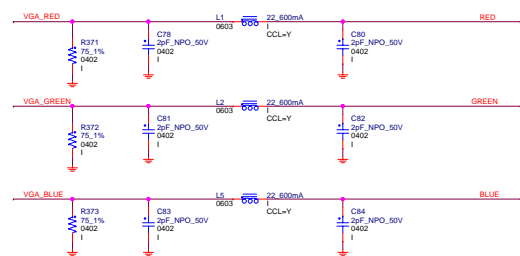
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Date: <b>Thursday, July 14, 2016</b>		Sheet: <b>42</b>		of: <b>62</b>	



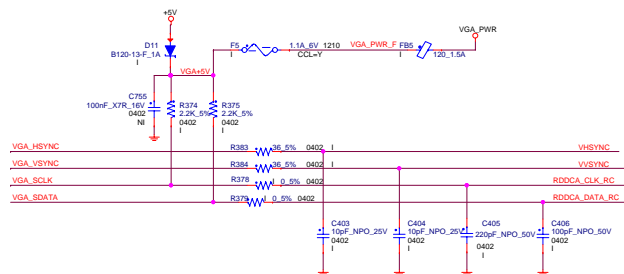
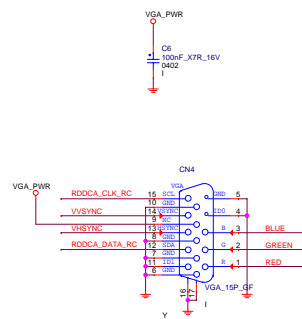
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Title <b>CARD READER</b>			
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Custom	TBD	0A	
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# VGA

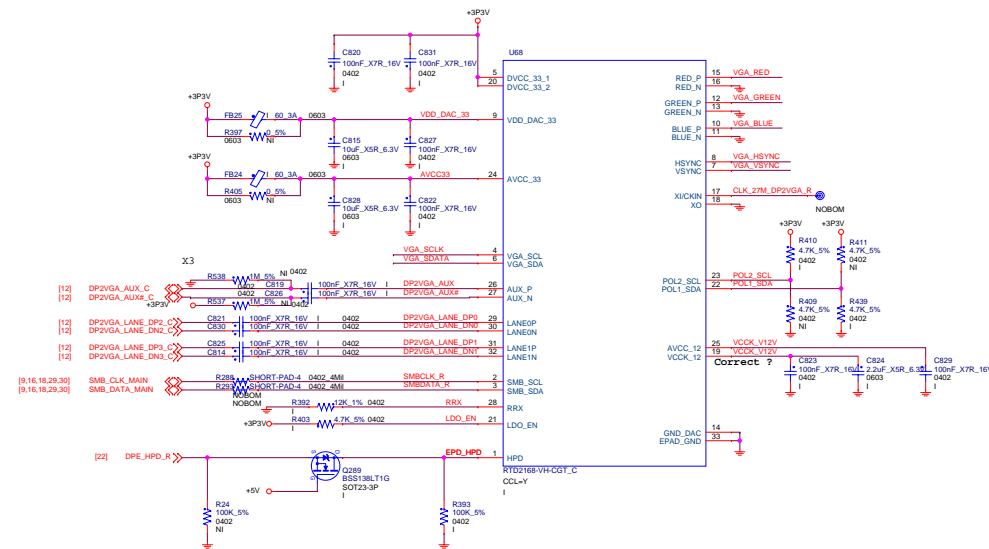


Place 150 ohm resistors close to filters (Cap/Ferrite-Beads)

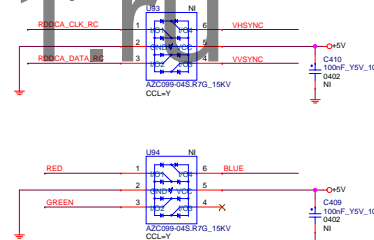


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## DP to VGA\_RTD2168

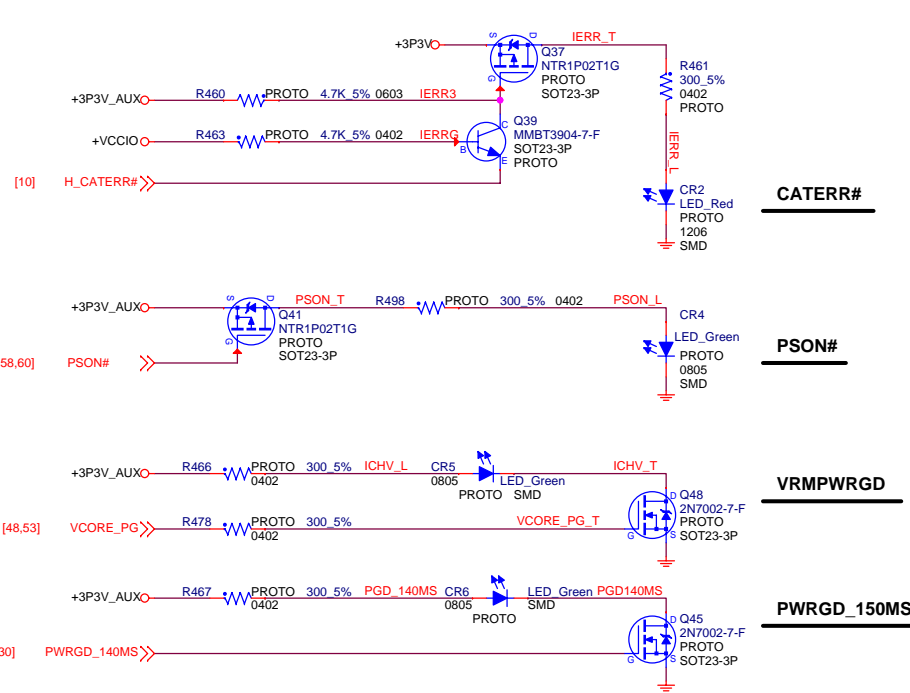


ESD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the ESD diode.



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Sheet: 44 of 62					
Rev: <b>0A</b>					



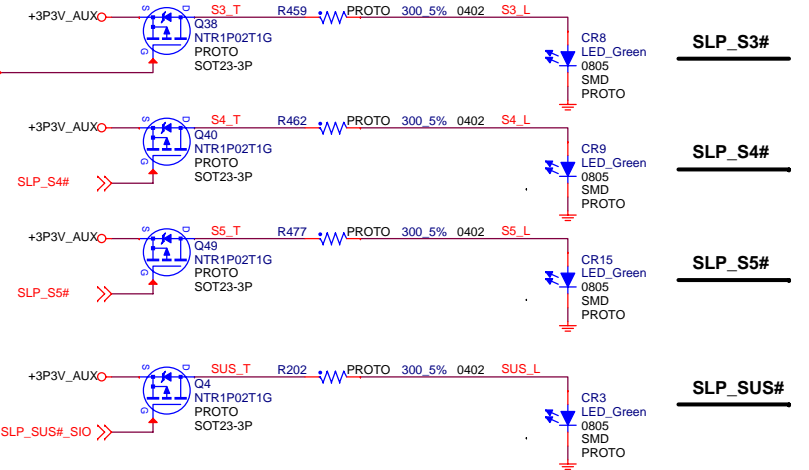
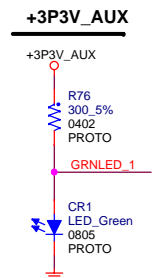
### PCA LED

[23,30,34,38,53,57] SLP\_S3#

[13,23,30,34,38,56,59] SLP\_S4#

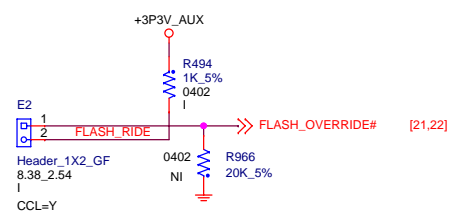
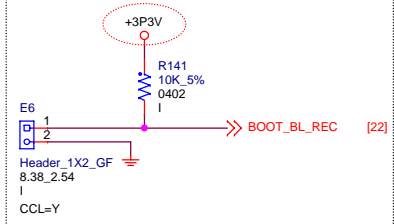
[23] SLP\_S5#

[30] SLP\_SUS#\_SIO



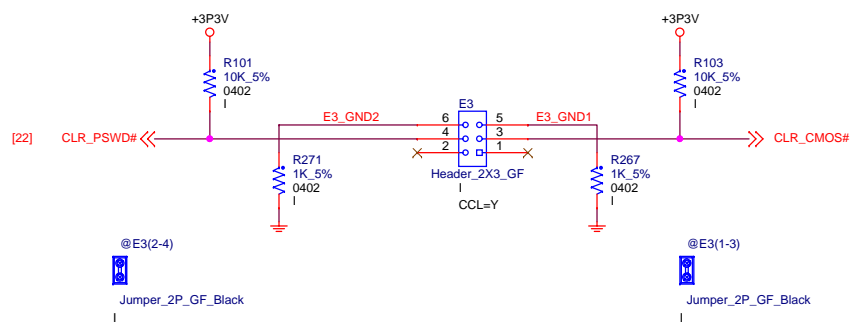
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### FLASH OVERRIDE (ME Disable)

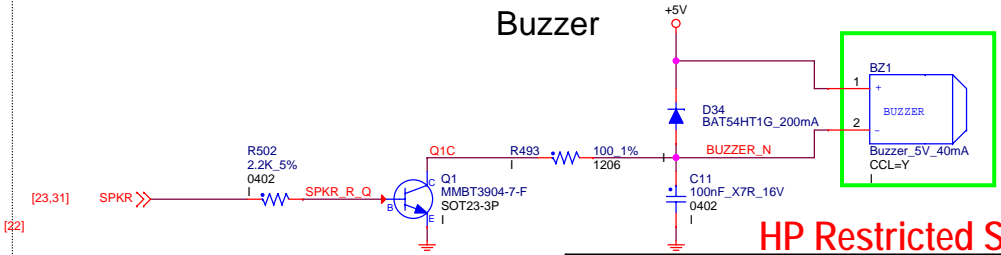


### CLEAR PASSWORD

### CLEAR CMOS



### Buzzer



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Size		Document Number			
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Rev		0A			

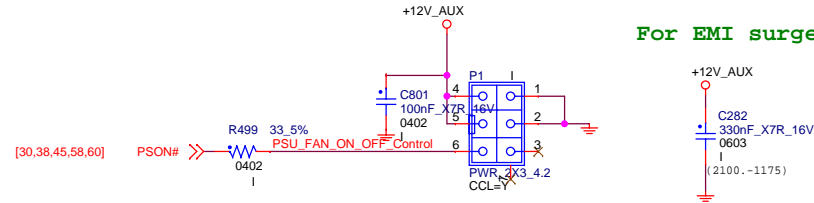
## Power Input Connector

PSON# is an active low that allows the power supply fan and trig the PSU to go down to power saving mode power supply. when the system is in S3/S4/S5

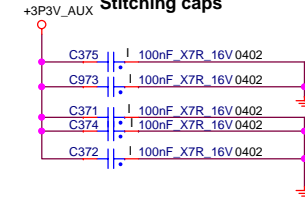
## EMI CAP

FXN EMI SUGGESTED PLACEMENT

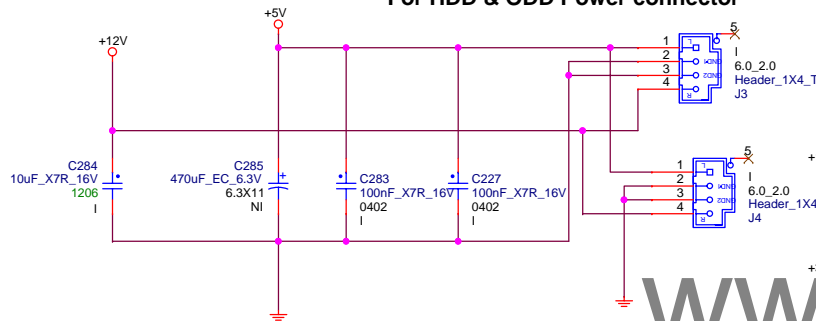
### For EMI surge issue



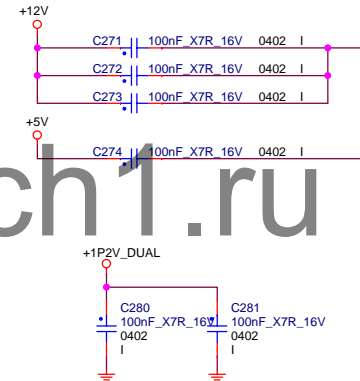
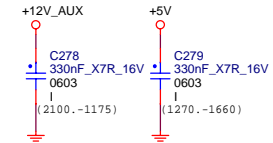
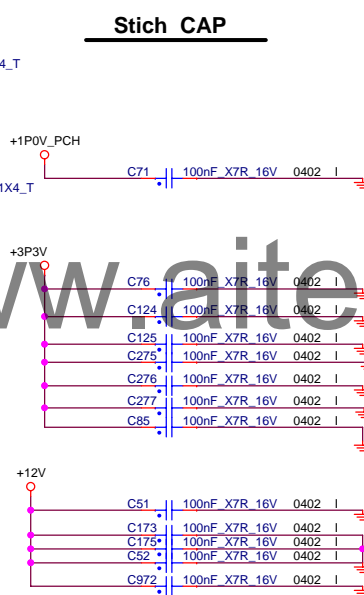
### Stitching caps



### For HDD & ODD Power connector

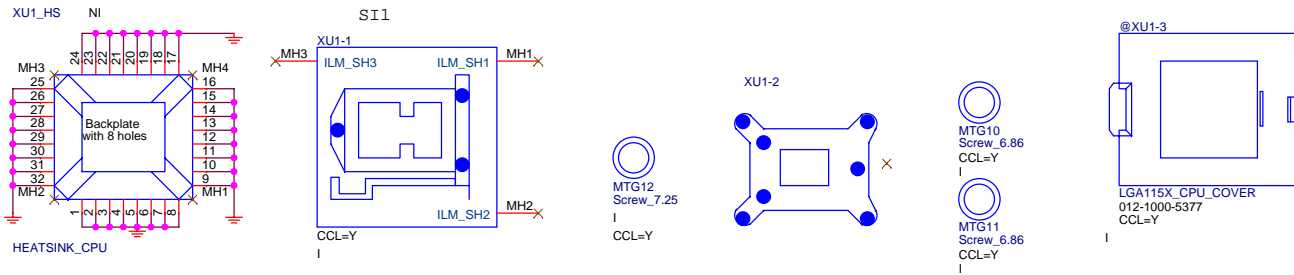


### Stich CAP



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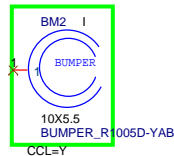
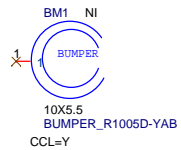
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Title <b>POWER INPUT &amp; EMI CAP</b>					
Size Document Number Custom TBD					Rev <b>0A</b>
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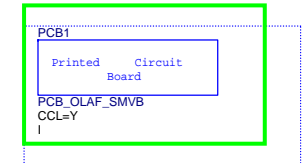
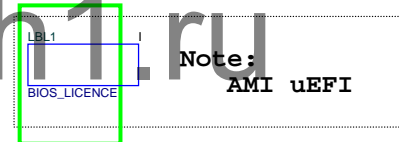
ILM & SCREWS

Licence Label

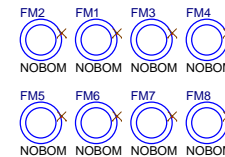
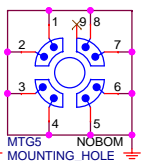
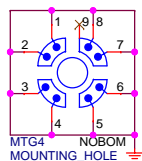
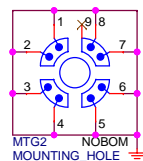
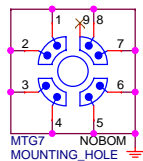
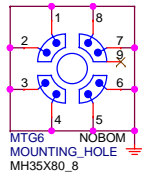
PCB



PV to SMVB(20160624):  
1.Change BM2 BOM from NI to I since SID requirement

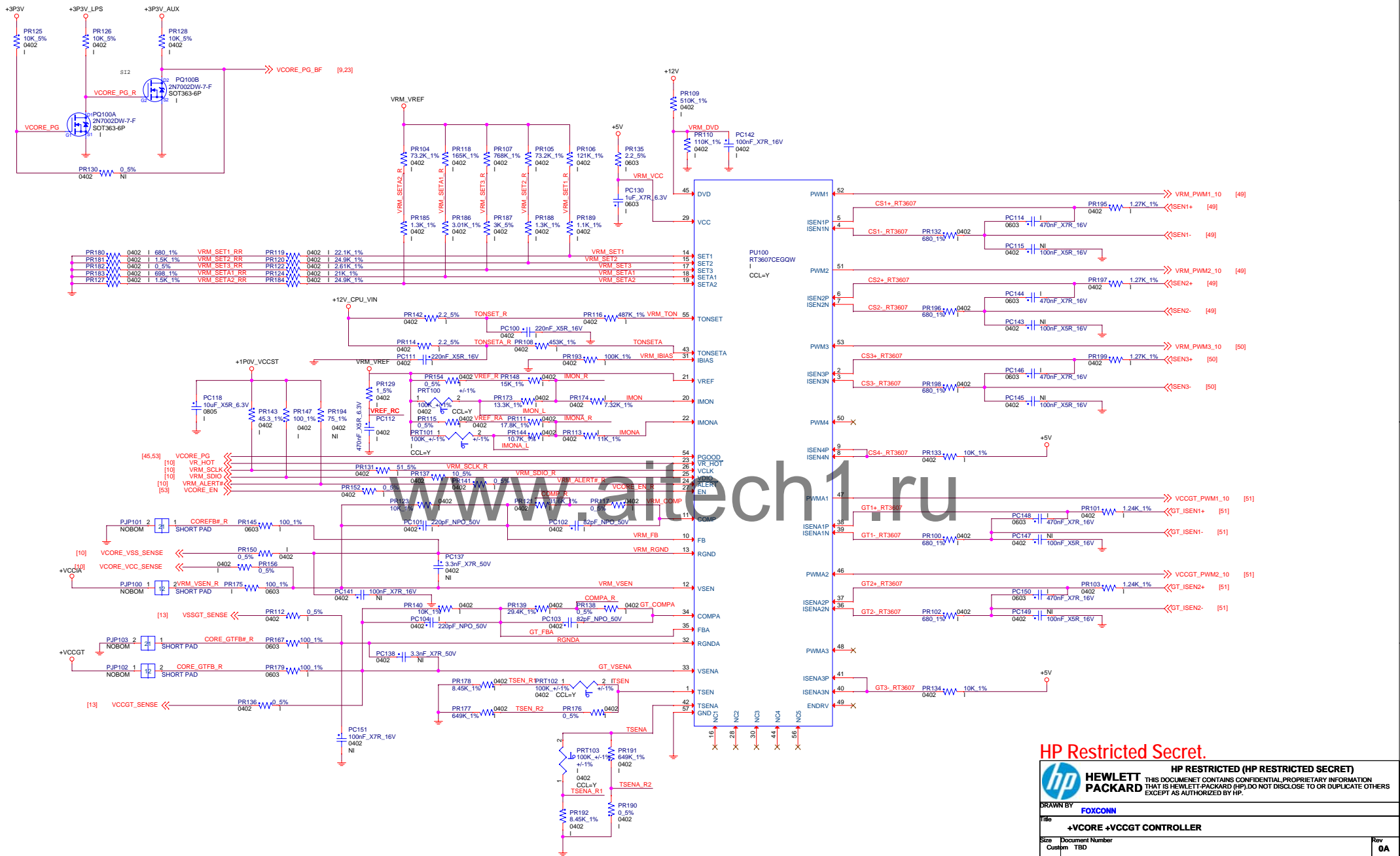


PV to SMVB(20160624)::  
1.Change PCB PN



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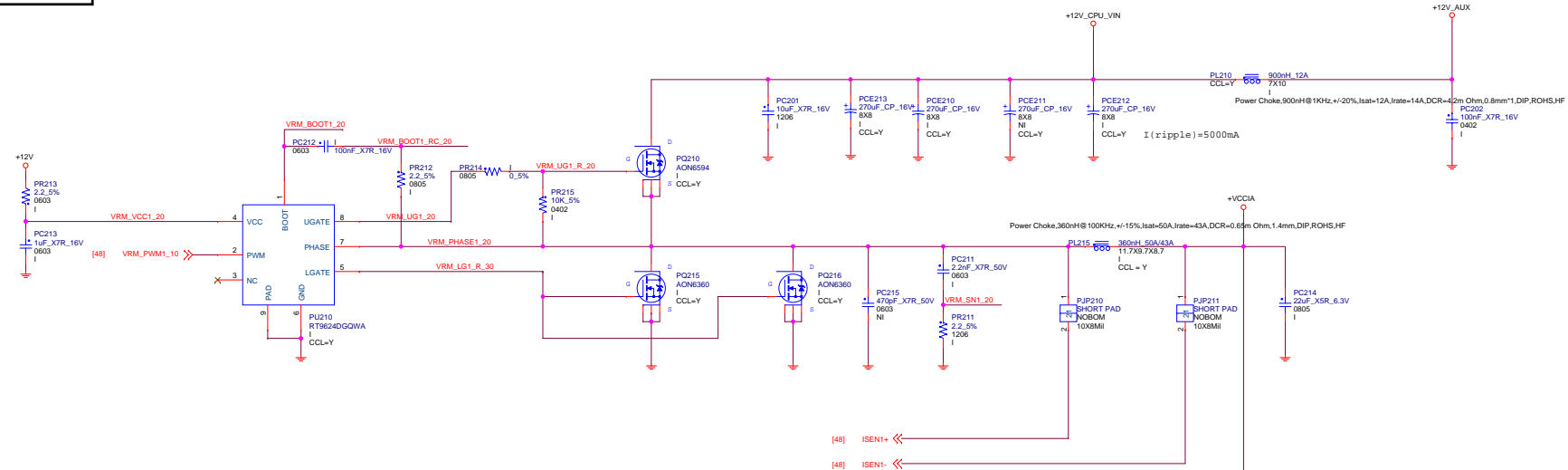


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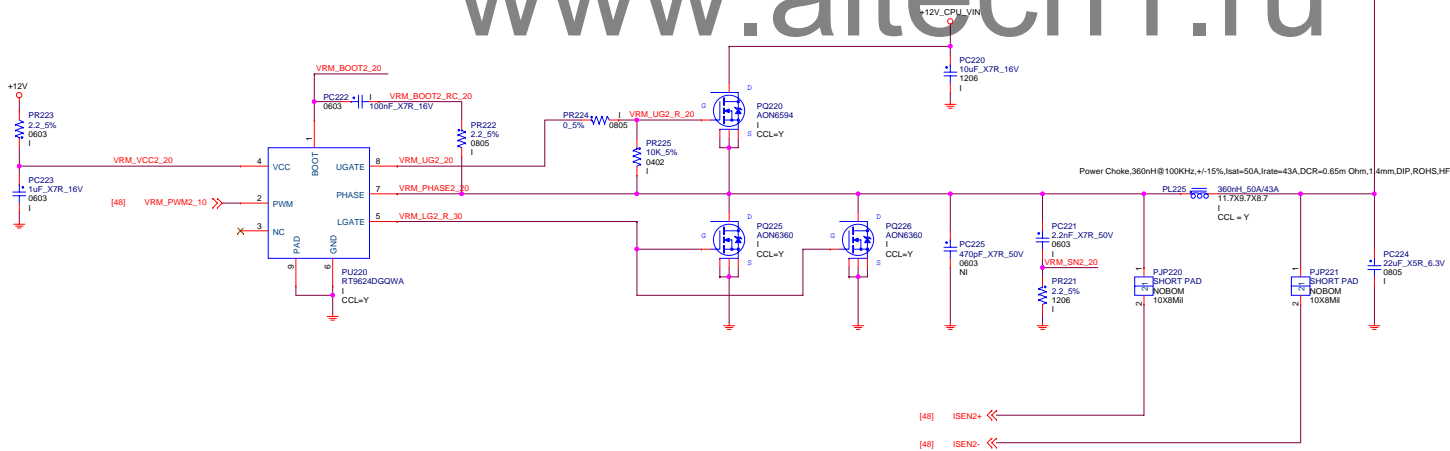
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<b>+VCCGT VCCGT CONTROLLER</b>			
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# VCORE PHASE1~2



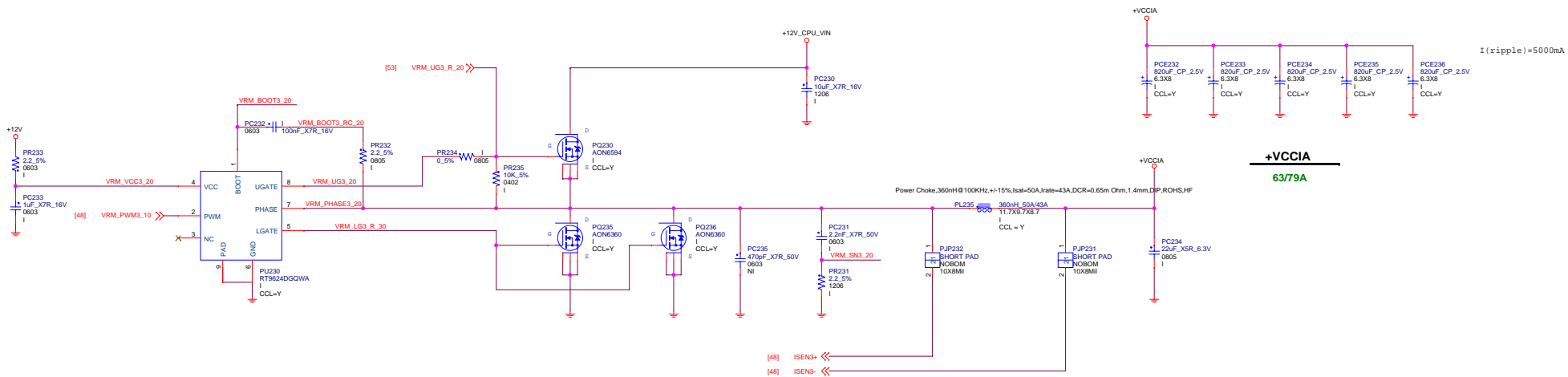
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File: <b>+VCORE phase1&amp;phase2</b>			
Site: <b>Custom</b> Document Number: <b>TBD</b>			
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## VCORE PHASE3



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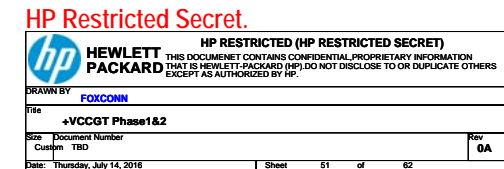
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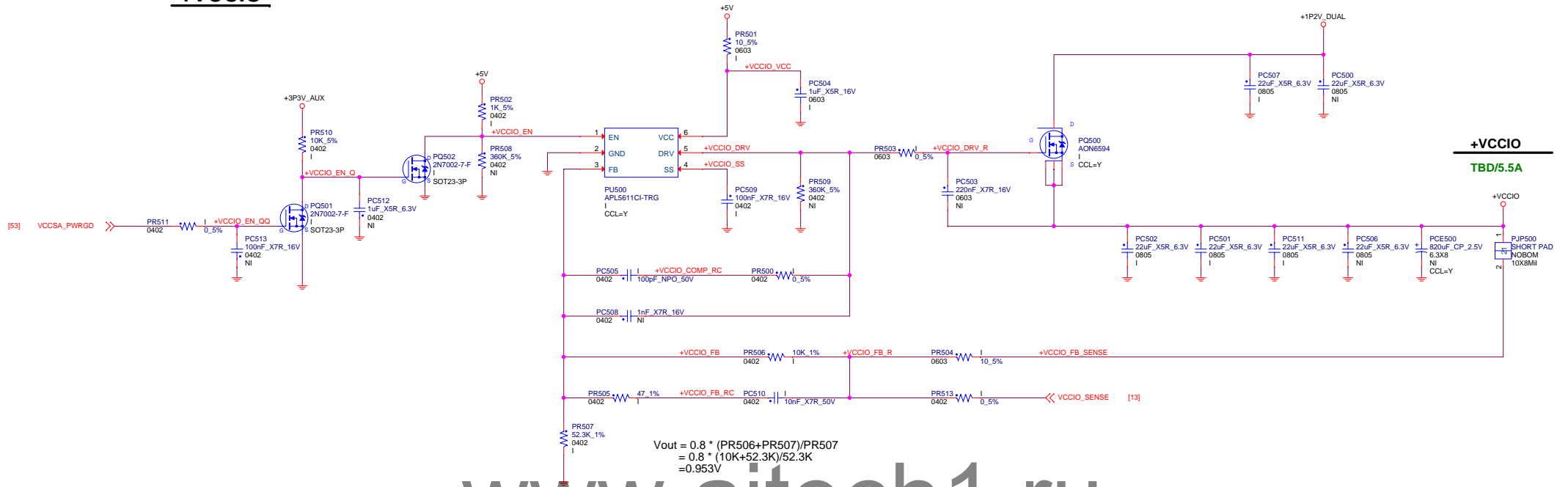
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Rev  
04

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**+VCCIO**

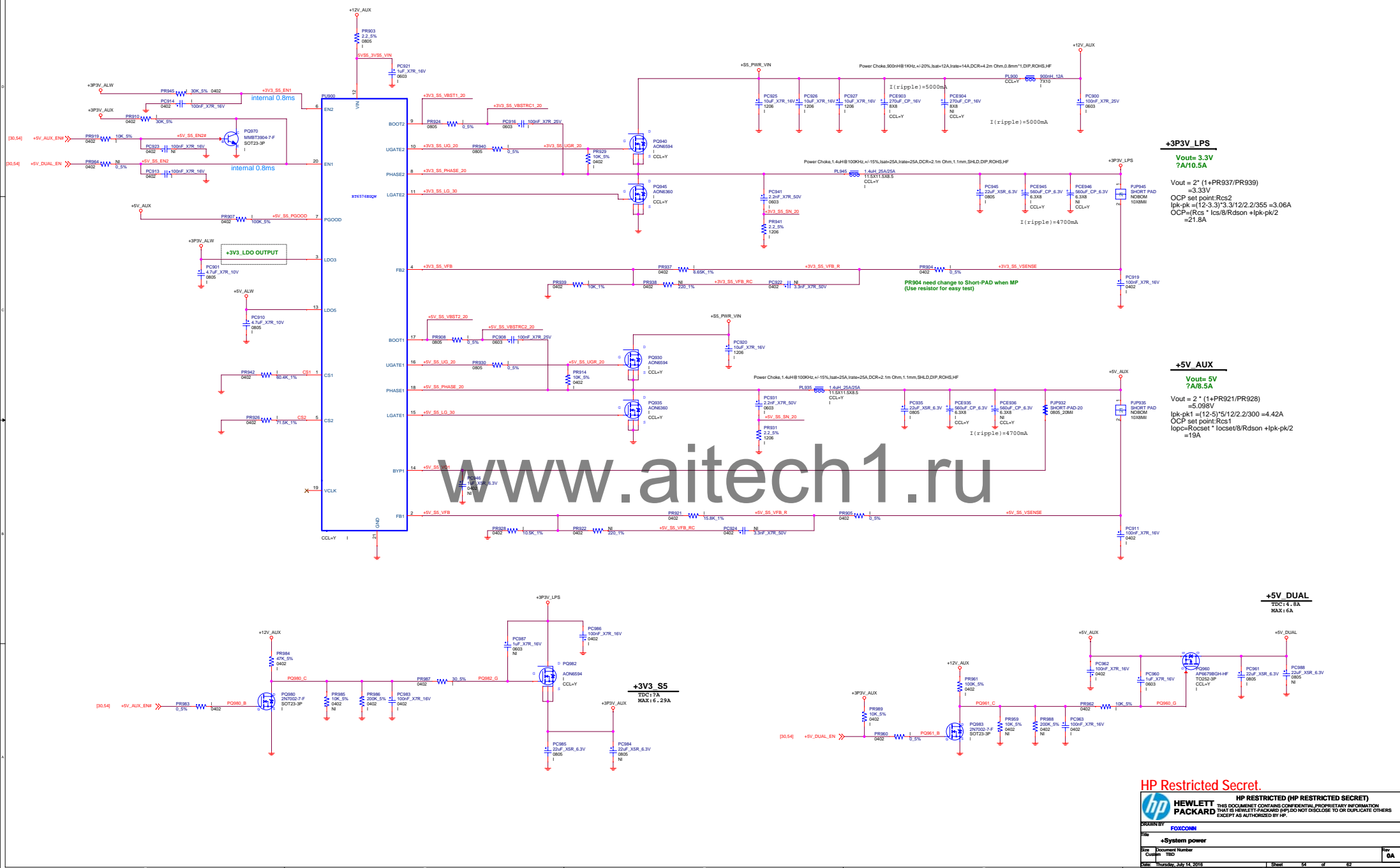


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+System po

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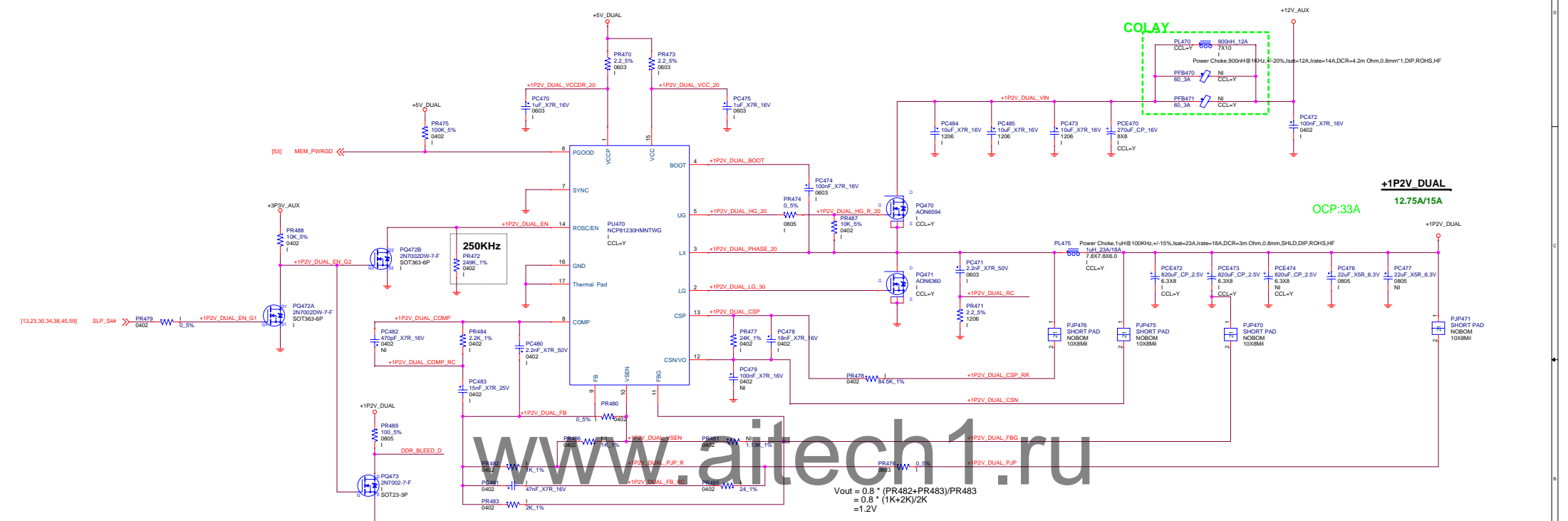
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Rev
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+1P2V\_DUAL POWER(DDR 4)



$$V_{out} = 0.8 \cdot (PR482 + PR483) / PR484$$
$$= 0.8 \cdot (1K + 2K) / 2K$$
$$= 1.2V$$

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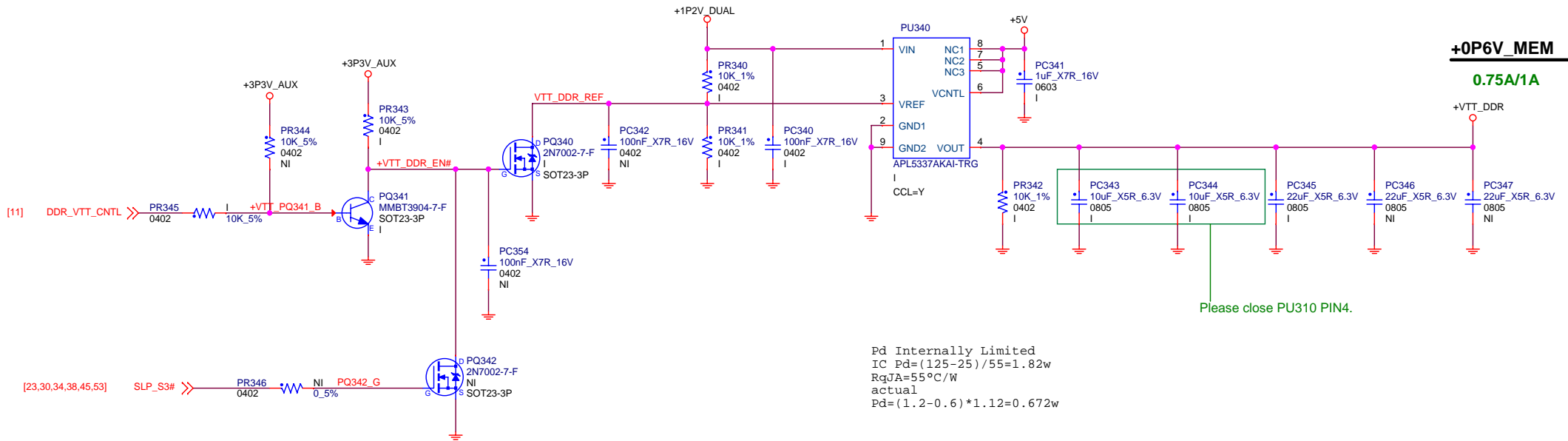
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## DDR\_VTT

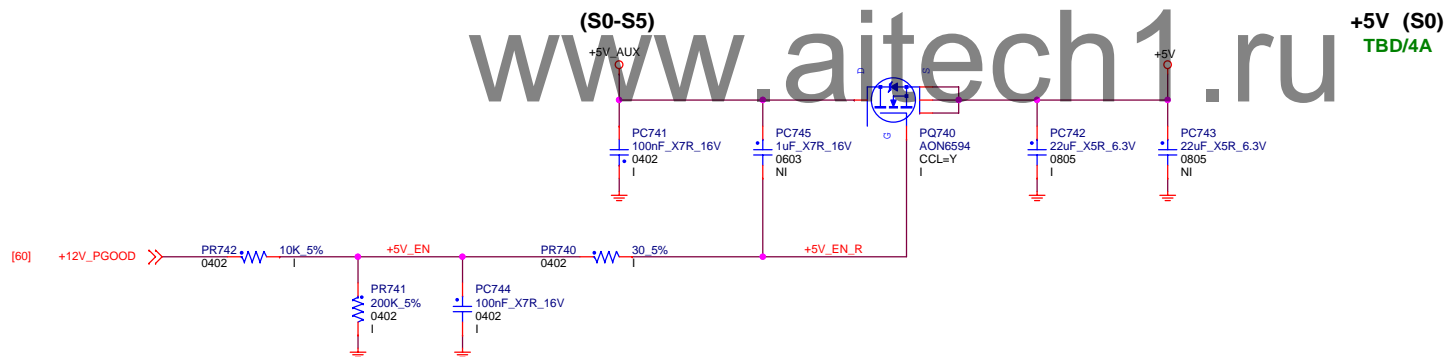
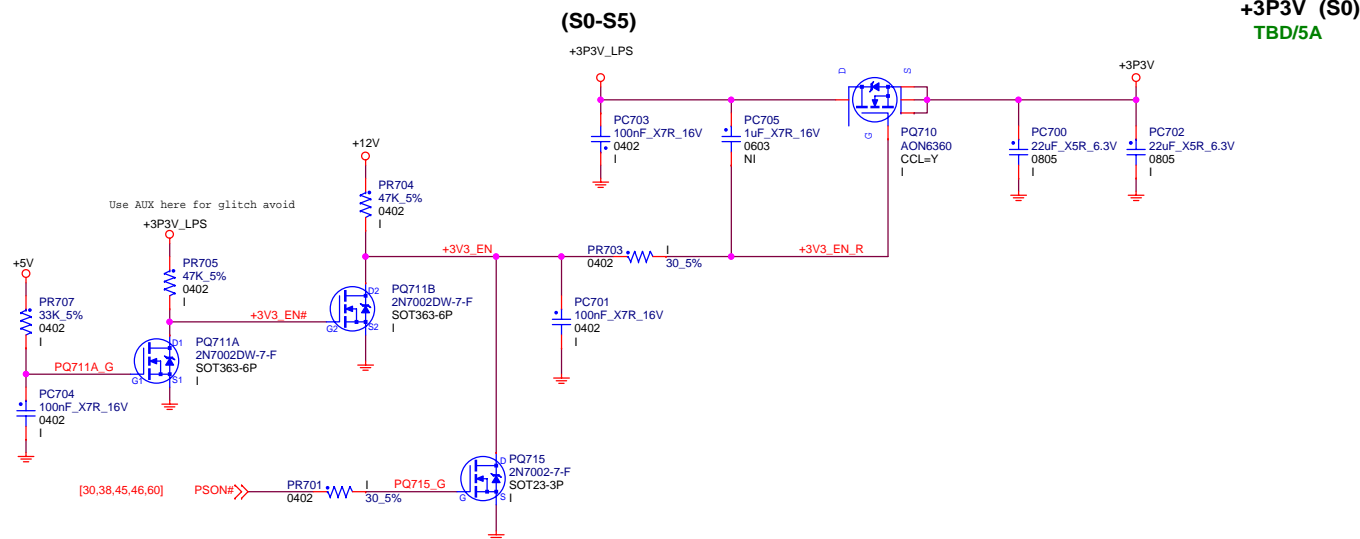


Pd Internally Limited  
IC Pd=(125-25)/55=1.82w  
RqJA=55°C/W  
actual  
Pd=(1.2-0.6)\*1.12=0.672w


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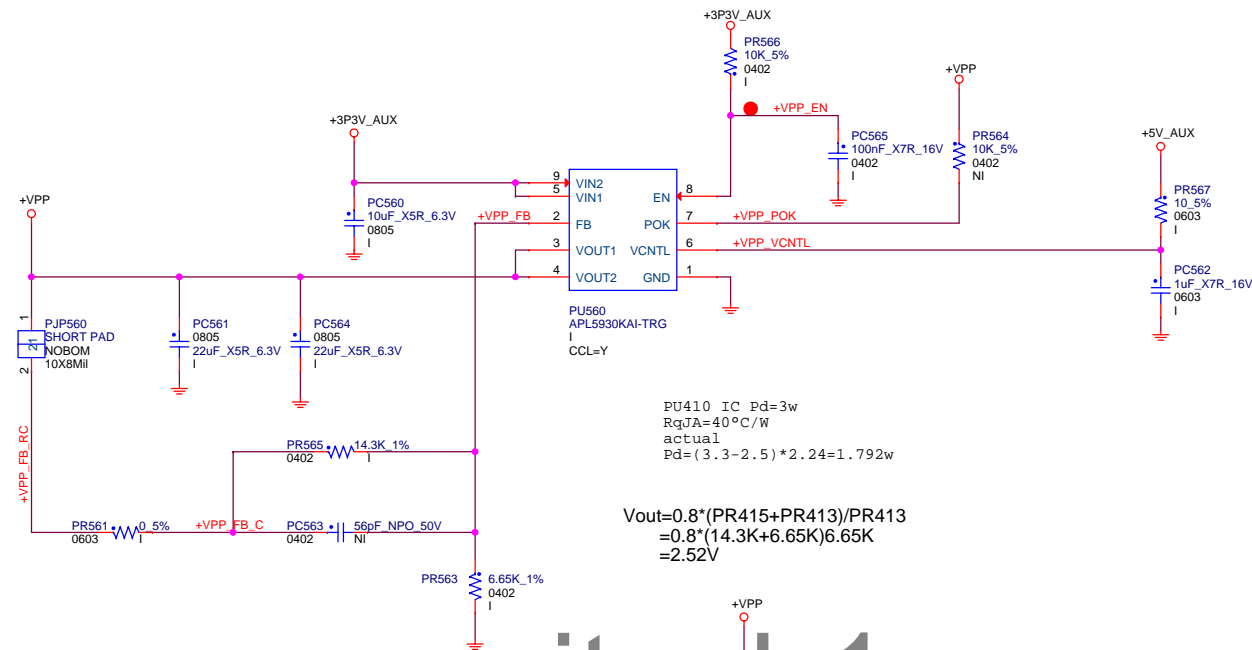
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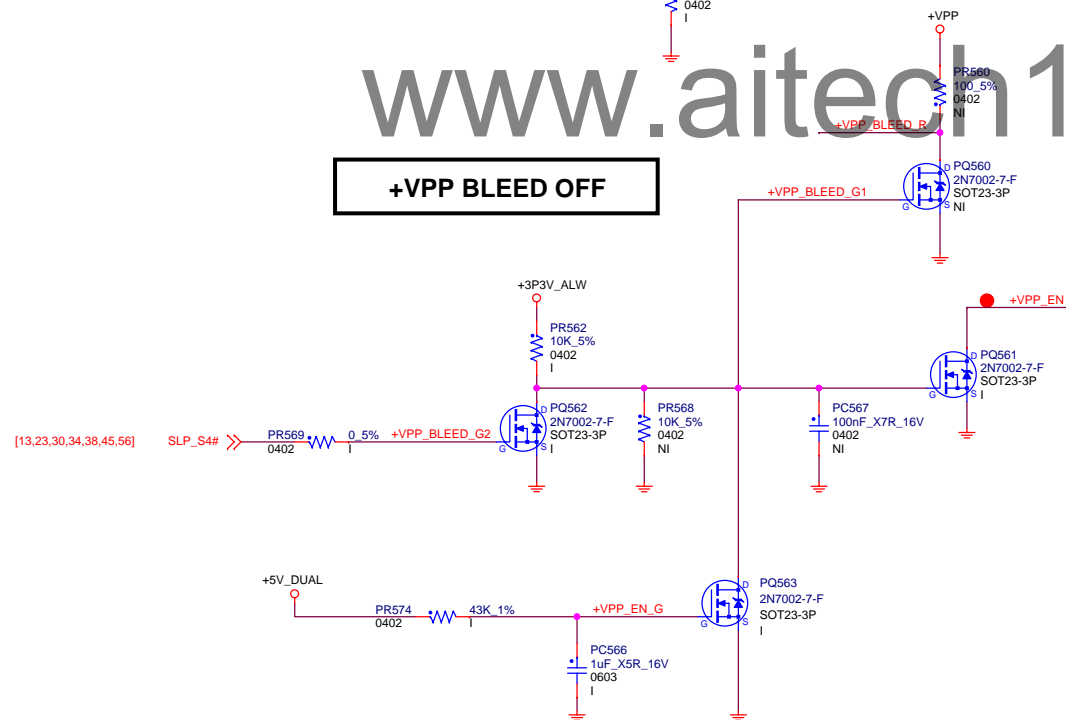
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Title <b>+5V&amp;+3V3</b>			
Size	Document Number	Rev	
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**+VPP**  
TBD/2.24A (DDR4)

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**+VPP BLEED OFF**



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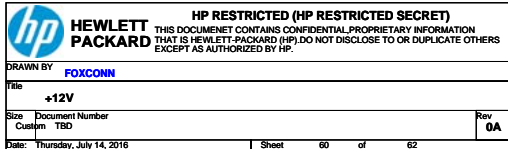
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PR754

[58] +12V\_PGOOD <<—

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 **HP REST**

## SI change List(EE Part)

20160217

- 1.Page23: Change R198 from I to NI and R193 from NI to I .Revision change from DB 00 to SI 01
- 2.Page 43: Change card reader connector height from 4.7mm to 5.4mm  
since front IO connector height matching issue
- 3.Page 47: Update PCB PN

20160229

- 1.Page23 Add R959 10ohm at PCH side for APU\_RST over shoot fail
- 2.Page23 Add R960 10ohm at PCH side for H\_PWRGOOD over shoot fail
- 3.Page30 Change SR58 from 33ohm to 22ohm to fix LPC\_GLAN\_RST# non monotonic issue
- 4.Page23 Change R336 from 22ohm to 33ohm to fix SIO\_RSMRST# non monotonic issue
- 5.Page23 Change R228 from 0ohm to 22ohm to fix SLP\_S3# non monotonic issue
- 6.Page31 Change AR44/AC63/AC25/AC26/AC27 from I to NI to reduce AUDIO Noise
- 7.Page22/39 Change SATA0/SATA1 connection order between PCH and SATA connector  
P62 connect with PCH SATA0, P63 connect with PCH SATA1.

20160305

- 1.Page31 Change AR11 pull high voltage from +3P3V to +3P3V\_DVDD  
fix +3P3V have 0.2V leakage voltage during S3/S4/S5 issue
- 2.Page30 Change SR247 value from 10K ohm to 8.2K ohm and  
SR247 pull high voltage from +5V\_ALW to +3P3V\_LPS to match PSU fan control signal
- 3.Page32 Change front AUDIO Combo Jack AJ2 PN from SINGATRON\_2SJ3082-031112F to  
SINGATRON\_2SJ3082-051111F to fix contact pin short length issue (length from 1.55mm to 2.0mm)

20160311

- 1.Page44 Change R378 from 33ohm to 0ohm  
C405 from 100pF to 220pF to fix RDDCA\_CLK\_RC non monotonic issue
- 2.Page44 Change R379 from 33ohm to 0ohm to fix RDDCA\_DATA\_RC non monotonic issue

20160314

- 1.Page29 Add USB Header for PCIEX1 card according new PCA spec
- 2.Page42 Change Rear USB from USB3.0X2+USB2.0X2 to USB2.0X4 according new PCA spec
- 3.Page36 Change SYS Fan from PROTO to I according new PCA spec
- 4.Page31/47 Change MTG1/MTG6 diameter from 3.96mm to 3.5mm according new request

20160315

- 1.Page41 Change F\_USB3\_1/F\_USB3\_2 from FOXCONN/UEA1117-44126-4H  
to fix JYEC\_UB1003F-B007-09A400B to fix ME matching issue
- 2.Page43 Change card reader from PROTO to I according new PCA spec

20160317

- 1.Page31 Remove AR10/AR13/AR14/AD58/AQ1 to  
Change Audio Mute function control signal from SIO GPIO to PCH GPIO.
- 2.Page24 Add R963 Proto 0 ohm to avoid MVB E1 Pin2 or E8 pin9  
PCH\_RTCRST# contact GND cause RTCRST during DT assembly.
- 3.Page37 Change LX2 from TXC\_9B25000013(Ta=70C) to TXC\_9B25000007 (Ta=80c)  
To improve LX2 thermal test margin
- 4.Page47 Reserved Bumper BM1/BM2 for SI phase since SID request

20160319

- 1.Page20 Adjust USB2 mapping for BIOS USB2 set up order optimization.  
USB2 port2 swap with port3 and port6 swap with port7.
- 2.Page43 Change RS4 from short pad to Fuse F6.
- 3.Page23 Change PCI\_EXP\_WAKE# pull high resistor from Lan side to PCH side.  
NI LR2 and add R964

20160406

- 1.Page41 Change Front\_USB3\_1/Front\_USB3\_2 footprint from USB3\_9\_516X650 to  
USB3\_9\_516X650\_T according to discussion with SID
  - 2.Page36 Change R553 from 33 Kohm to 10K ohm to optimize system Fan design
  - 3.Page37 Change LX2 back to TXC\_9B25000013(Ta=70C) follow the newest thermal test report
  - 4.Page43 Change card reader ESD U13/U14 from I to NI since the newest PCA spec.
  - 5.Page30 Change SR204 from I to NI since the signal have two pull high resistor
- 20160408
- 1.Page31 Change AC32/AC33/AP1 PROTO to NI according new PCA spec
  - 2.Page34 Change TPM module from PROTO to NI since SI have no build plan

20160412

- 1.Page38 Change LC19/LC20 from NI to I for LAN surge
- 2.Page39 Change LU5/LU6 from I to NI for LAN surge

## SI change List(DC Power Part)

20160217

1. PQ711 and PQ754 change from 2N7002DWA-7-F to 2N7002DW-7-F
2. Add PR762 0.5% for debug
3. PR962 change from 2.2K to 10K for optimize +5V\_DUAL's softstart
4. PC960 change from NI to I for optimize +5V\_DUAL's softstart
5. PR753 change from 7.5K to 470K for optimize +12V's softstart
6. PR755 change from 10K to 470K for optimize +12V's softstart
7. PC751 and PC753 change from I to NI for optimize +12V's softstart
8. PL606 change footprint from L3131\_T\_R83X276 to L3131\_T\_R83X276\_MVB

20160308

1. PC481 change from 100nF to 47nF for +1P2V\_DUAL's PM&GM
2. PR113 change from 13.3K to 11.8K for Imon optimize
3. PR195,PR197,PR199 change from 1.43K to 1.24K for Imon optimize
4. PR101,PR103 change from 1.43K to 1.21K for Imon optimize
5. Add PR990 and PQ967A to fix VCCST\_PWRGD\_IV drop

# Change List

## PVT change List(EE Part)

20160509

- 1.Page23: Change R196/R193 from I to NI and R198/R168 from NI to I .Revision change from SI 01 to PV 10
- 2.Page 47: Update PCB PN
- 3.Page23: Change E7/E16/@E16(1-2) from PROTO to I,R351 from MP to NI for PV phase CDC project BOM rule

20160521

1. Page30: SUS\_PWR\_ACK# add SR255 33ohm to fix under shoot issue
2. Page 22: Add R965 for PCH GPIO GPP\_I7 connect with FLASH\_OVERRIDE# to support Intel ME/TXE FW Update capability.
3. Page 45: Reserved R966 20Kohm for FLASH\_OVERRIDE# pull down

20160526

1. Page31: Reserved AC68/AC69/AC70/AR81/AR82/AR83 connect AGND and GND for AUDIO debug

## PV change List(DC Power Part)

20160516

1. Page48: VCCIA:PR195,PR197,PR199 change from 1.24K\_1% to 1.27K\_1%  
VCCGT:PR101,PR103 change from 1.21K\_1% to 1.24K\_1%  
PR113 change from 11.8K\_1% to 11K\_1%

## SMVB change List(EE Part)

20160624

1. Page9: Change P4 footprint from HMS2X30CZ to HMS2X30CZ\_MVB\_NP Add sloder masker on XDP pin
2. Page23: Change Board version from PV(010) to SMVB(011)  
R193 change from NI to I  
R198 change from I to NI
3. Page34: Change PV phase debug component from I to PROTO  
Change E7 LPC debug header BOM from I to PROTO  
Change E16 BOM from I to PROTO  
Change @E16(1-2) BOM from I to PROTO  
Change R351 BOM from NI to MP
4. Page47: Change PCB PN
5. Page47: Change BM2 BOM from NI to I since SID requirement

20160627

1. Page32: AJ2 Change MFG PN from SINGATRON\_2SJ3082-051111F to SINGATRON\_2SJ3082-066112F  
Note: Vendor only change material package and mechanical tolerance spec

20160708

1. Page33: Change CR14/CR18 from Liteon LTW-42NDP4H218 to Liteon LTW-42NDQ9H218 for LED brightness issue


20160711

1. Page38: Change LJ2 from FOXCONN\_JFM38U1G-FPV2-4F to SPEEDETECH\_RUA2JA-4JR3-BE0-0H for RJ45 offset issue

20160714

1. Page37: L69 from MAGLAYERS/MLCF-252018-2R2K to TAI-TECH/SWF2520CF-2R2K  
since MAGLAYERS/MLCF-252018-2R2K not provide ROHS document on time

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DRAWN BY <b>FOXCONN</b>					
File <b>CHANGE LIST</b>					
Size Document Number					
Cusom TRD					
Rev <b>0A</b>					
Date: <b>Thursday, July 14, 2016</b>					
Sheet <b>61</b> of <b>62</b>					